USER MANUAL

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LING DYNAMIC SYSTEMS

SERVICE INFORMATION

CALIBRATION & MAINTENANCE
DIGITAL SINE CONTROLLER
MODEL DSC-8 Mk II
PART No. 878502

CONTROLLED DOCUMENT

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Amendments

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INSTRUMENT CALIBRATION & MAINTENANCE MANUAL

AMENDMENT RECORD

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CIRCUIT DIAGRAMS

958120	Display P.C.B.	- SC01
959190	C.P.U. P.C.B.	- SC02
958140	Sine Generator P.C.B.	- SC03
959200	Compressor P.C.B.	- SC04
959210	Feedback P.C.B.	- SC05
958170	Metering P.C.B.	- SC06
958180	Status Display P.C.B.	- SC09
958610	Charge Amplifier P.C.B.	- SC10
959230	GPIB Interface	- SC11 & SC12
958750	Keyboard	
958660	Remote Control Unit	
959180	Schematic Wiring Diagram	

SECTION 1 - INTRODUCTION

This manual gives a technical description, test and calibration procedure for the Digital Sine Controller DSC8. A basic knowledge of electronics is assumed. A dollars sign preceding a number indicates that it is in hexadecimal.

Operating instructions are given in the Operator's Manual Part No. 875501.

Always disconnect the unit from the mains supply before removing components or internal connexions. The plug-in printed circuit boards can be fitted in the Unit in any order although the prefered positions are marked on the Motherboard. The boards must be fitted with their component side towards the lefthand (power supply) side of the unit. The unit contains devices which are sensitive to electrostatic charge and may be damaged if the usual precautions are ignored.

WARNING

The unit contains a switched mode power supply and CRT drive card. Some components in these assemblies are at a high potential whilst the Unit is operating and for some time after it is switched off. After disconnexion from the a.c. mains supply allow 5 minutes for all capacitors to discharge before handling these assemblies.

SECTION 2 - SPECIFICATION

Frequency Range	1 Hz to 6500 Hz by 0.1 Hz increments.
Frequency Stability	+/- 50 ppm / deg C.
Frequency Display	0.1 Hz resolution, updated 4 times/second.
Sweep Modes:	
Linear Sweep	0.1 to 99 Hz/s.
Logarithmic Sweep	0.01 to 9.9 oct/min.
Number of Sweeps	1 to 255, or continuous.
Manual Sweep	Normal and Fast rates.
Fixed Sine Output:	5V rms. T.H.D. < 0.1% 20 Hz to 6500Hz (measurement bandwidth 20kHz) Signal to noise ratio 70dB
Servo Output:	Differential output, 7V rms at 0dB T.H.D < 0.1% 20 Hz to 5000 Hz (measurement bandwidth 20kHz)
Compression	0dB to 99.9 dB, resolution 0.1 dB.
Compression rate	0.5, 1.0 or 4.0 dB/s/Hz maximum selectable from 10 to 999 dB/s
Control Range	See fig 1 and fig 2. Up to eight control levels per test may be specified.

Control Accuracy (Refered to normalised g input), Optimum sweep and compression rates.

Acceleration	+/- 0.2 dB	5 Hz to 5000 Hz
	+/- 0.4 dB	5000 Hz to 6500 Hz
Velocity	+/- 0.5 dB	1 Hz to 5 Hz
	+/- 0.2 dB	5 Hz to 1000 Hz
	+/- 0.5 dB	1000 Hz to 2000 Hz
Displacement	+/- 1.0 dB	1 Hz to 5 Hz
	+/- 0.3 dB	5 Hz to 500 Hz
	+/- 1.0 dB	500 Hz to 2000 Hz

Metering	Auto ranging, 3 1/2 digit scale, updated 4 times/second. Measured parameter automatically corresponds to programmed parameter, with manual over-ride. Measurement of channel 1 or channel 2 level. R.M.S. sensing, peak calibration.

Metering Accuracy (Refered to normalised g input).

Acceleration	+/- 1%	20 Hz to 2000 Hz
	+/- 3%	1 Hz to 6500 Hz
Velocity	+/- 3%	1 Hz to 5 Hz
	+/- 2%	5 Hz to 2000 Hz
	+/- 3%	2000 Hz to 6500 Hz
Displacement	+/- 5%	1 Hz to 5 Hz
	+/- 3%	5 Hz to 1000 Hz
	+/- 5%	1000 Hz to 2000 Hz

Control Signal Input (channel 1)

Accelerometer	Charge amplifier. Transducer sensitivity 1.0 to 99.9 pC/g. Gain stability better than 1% per 10nF change of input capacitance. Gain accuracy +/- 1.5% at 400 Hz, - 3% at 1 Hz and 6500 Hz.
Normalised Input	10 mV/g or 100 mV/g

Metering Signal Input (channel 2)

Normalised Input	10 mV/g or 100 mV/g (the same as channel 1).

XY Plotter Drive	Derived from displayed frequency and acceleration (CH1 or CH2). Available only whilst PLOT indicator is illuminated. Accuracy +/- 2% or 5mV.
Frequency	log or linear, corresponding to sweep selected. log: 2.56 V/decade linear: dependant on highest frequency in test 1000Hz or above, 1mV/Hz, 10Hz resolution; less than 1000Hz, 10mV/Hz, 1Hz resolution; less than 100Hz, 100mV/Hz, 0.1Hz resolution.
Acceleration	log 2.56 V/decade of acceleration 10.2V full scale equivalent to 999.9g.
Pen Lift	Change-over relay contacts allow plotting of first sweep of test.
Calibration Mode	Fixed frequency of 44.7 Hz. Uses level of 2.5 mm peak - peak, equal to 10g peak.

System Protection

Control Signal Detector	Operates at commencement of test if, at 20 dB of compression, the control signal is not within 14 dB of the programmed level. Operates during test if the control signal is not within 3 dB of the programmed level. (Monitoring is selected during test set-up)
Maximum Output Detector.	Operates if minimum compression, set by Output Limit, is reached.

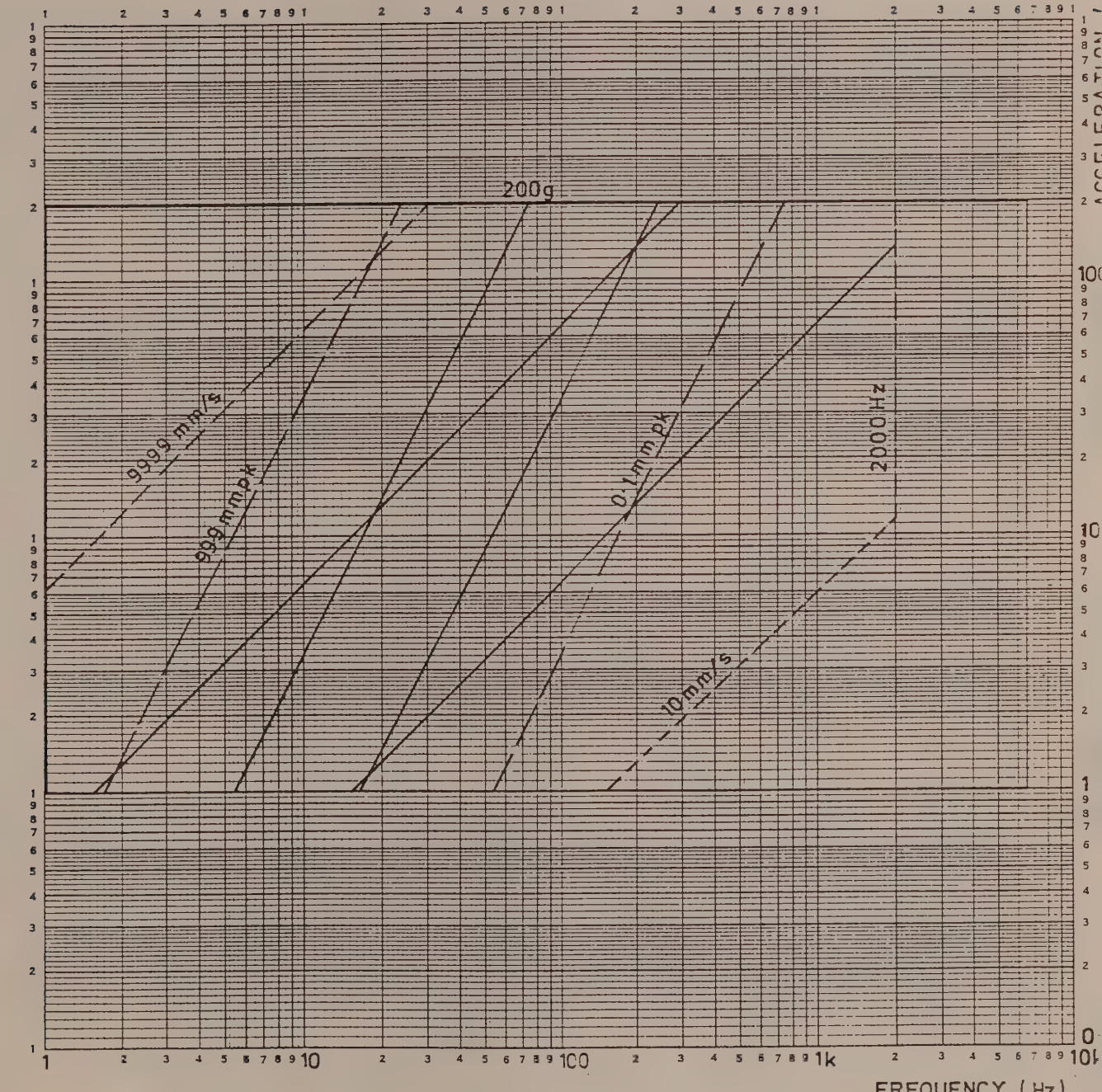


FIG 1

CONTROL CHARACTERISTICS

Normalised Level = 10 mV/g

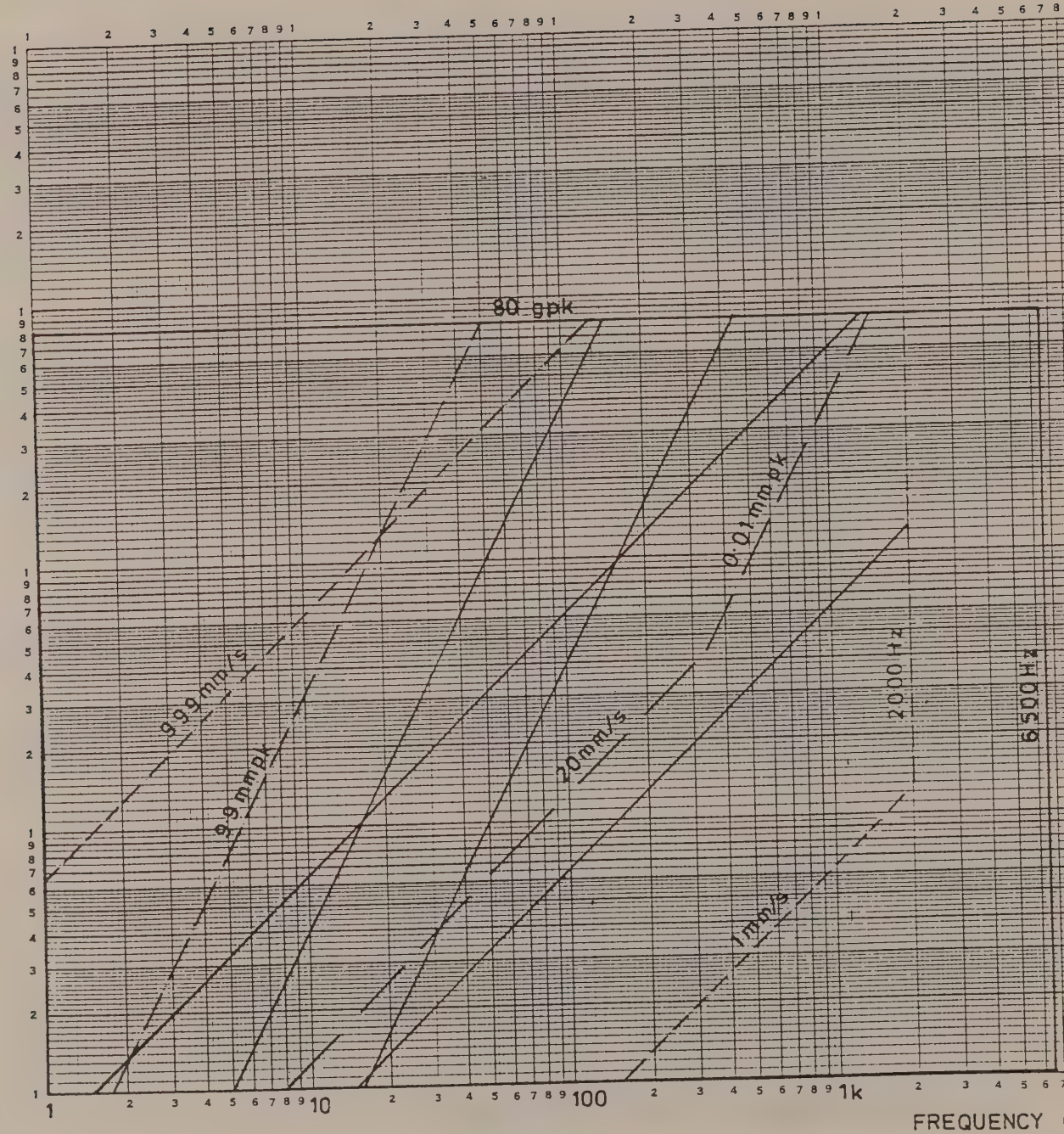


FIG 2
CONTROL CHARACTERISTICS
Normalised Level = 100mV/g

External Controls	Remote Abort. External contacts close to abort test. Remote Start/Stop. External contacts open to Start, & close to Stop test. Start/Shutdown controls. Relay contacts close on commencement of test, and open on completion or shutdown.
Remote Control Unit	Frequency display (1 Hz resolution) and sweep direction indication. Duplicates front panel START, HOLD, REV, STOP and ABORT keys.
Test Program Storage	Data for eight tests is stored in battery powered memory. Storage time 5000 hours typical
GPIB Interface Option	IEEE 488-1978 standard remote control. Interface functions:- SH1, AH1, T6, L4, SR1, RL2, PP2, DC1, DT0, C0, E1.
General	
Power Requirements	90 - 132V or 180 - 264V 50/60 Hz 100 W.
Operating temperature	0 to 35 deg C ambient.

SECTION 3 - PROCEDURE UPON RECEIPT

3.1 Inventory

The DSC8 is dispatched with the following items:-

- Remote Control Unit
- Instruction Manual
- Rack Mounting Brackets (2 off)
- Mains Supply Socket
- Fuses, 2A (2 off)
- 15 Way D Range Connectors (2 off)
- BNC Shorting Plug
- BNC Plugs (5 off)
- Keys (2 off)

3.2 Installation

Remove the equipment from its packing box. Should the equipment need to be returned to the factory for service or re-calibration this packing should always be re-used.

The DSC8 may be used free standing or mounted in a 19 inch rack. In either case air must be allowed to flow freely through the ventilation slots in the bottom panel and the fan aperture in the rear panel.

When mounting the unit in a 19 inch rack, remove the trim strip from each side and replace it by a rack mounting bracket.

The rack mounting brackets are for location ONLY and must not be used to support the weight of the unit.

THE MAINS SELECTOR SWITCH MUST BE SET TO THE CORRECT VOLTAGE BEFORE CONNECTING THE DSC8 TO THE SUPPLY.

SECTION 4 - TECHNICAL DESCRIPTION, TEST & CALIBRATION

4.1 Introduction

The technical description of each printed circuit board is followed by its test and calibration procedure. The test and calibration procedures are intended to verify that the unit is operating within its specification. It may also assist in locating a fault but due to the nature of the Unit, a fault on one board may prevent the testing of the other boards. Similarly, the testing of the interlock and remote control functions on the C.P.U. - P.C.B. requires the other boards to be operational.

4.2 Test Routine

The Compressor, Feedback and Metering boards contain a number of programmable gain stages. To simplify the testing of these a routine is included in the Unit which enables the operator to write pre-determined data to these stages via the front panel keyboard.

To enter the Test Routine, press the 'LDS' logo on the keyboard followed by the unmarked key immediately above the CHANNEL key. (There are two unmarked keys filling the space between the PAGE and CHANNEL keys.) When required, the Test Routine should be entered directly after switch-on or Reset, pressing any other keys will inhibit entry. The section of the Unit to be tested is specified by pressing one of the digits from 0 to 9. The list of data values required for that section is then stepped through by repeatedly pressing the ENTER key. If it is necessary to go back to a previous data value the DELETE key should be pressed. The address of the section being tested and the data written to it is shown on the CRT display. To exit from the Test Routine, set the key switch to NORMAL and press the PROGRAM key.

Table 1. Key Functions In Test Routine

Key	Function
LDS Logo + blank key above CHANNEL	Enter Test Routine. (Initially set up for test of section 0.)
0	Test SC 04 Normaliser
1	Test SC 04 Plotter X - axis drive
2	Test SC 04 Plotter Y - axis drive
3	Test SC 05 Integrators
4	Test SC 05 Range gain
5	Test SC 05 Level gain
6	Test SC 05 r.m.s. to d.c.
7	Test SC 06 Integrators
8	Test SC 06 Range gain
9	Test SC 06 r.m.s. to d.c.
ENTER	Advance to next data values in current section
DELETE	Step back to previous data values in current section
PROGRAM	Exit from the Test Routine

4.3 Test Equipment Required

Oscilloscope — Bandwidth 5MHz sensitivity 5mV/cm (ideally memory or storage for use at low frequencies).

Digital Voltmeter — a.c. and d.c. ranges up to 20 volts. Resolution 0.1 mV. Accuracy +/- 0.2%. True r.m.s. sensing. Frequency range 1Hz to 10kHz.

Sine Wave Oscillator — Frequency range 1Hz to 10kHz. Distortion less than 0.1%. Maximum output 7V r.m.s.

Timer Counter — To measure frequency (or period) from 0.1Hz to 6500Hz with an accuracy of +/- 0.01%.

Distortion Analyser — 20Hz - 6.5kHz range, 20kHz bandwidth.

Continuity Tester

Capacitors	1nF +/- 0.5% and 10nF +/- 20% each fitted inside a metal box connected between the centre conductors of a microdot and BNC socket fitted to the box. The screens of both sockets should be in contact with the box.
Connecting Leads	As required.
GPIB Controller	IEEE 488 1978 std. (required for units fitted with GPIB option only).

4.4 Display P.C.B. SC 01 Circuit Diagram 958120

The CRT display is controlled by IC21, type R6545. The sixteen registers in this device are located at the addresses $9000 to $900F. The device is set up to display characters which are eight dots wide and twelve dots high, 40 characters per line, and 24 lines per page.

The information to be displayed is stored in IC3 and IC5 for the Menu page or IC4 and IC6 for the Metering page. In addition the character may be displayed in normal or reverse video, dependant upon the output of IC7 a high output giving reverse video display.

The display RAM, IC3 - 6, is addressed by IC21 or by the system address bus, switching of the address lines being performed by IC17,18 and 19. IC25 generates the dot clock frequency of 6.5MHz. This is divided by eight to give the character clock rate which controls IC21 (pin 21).
During the display period IC21 addresses consecutive memory locations in RAM. The data stored in RAM, combined with the address of the current row (or line) of the character which is being scanned on the screen forms the address for a PROM, IC1 or IC2. The PROM contains the eight bit dot pattern to be displayed as the current row. This is loaded into the shift register IC14 or IC15 and shifted out at the dot clock rate. If the character is to be displayed in reverse video the video signal is inverted in IC13 (pin 11 output). The flashing cursor is obtained in a similar way by inverting the video signal at a blink rate controlled by IC21 (pin 19).

When it is required to update the information for display the system bus addresses the display RAM. The $\overline{V}$ sync output from IC21 is tested by IC23 pin 39 on the CPU P.C.B. and is used to synchronise the updating to the display flyback period.

Display P.C.B. SC 01 Test and Calibration

There is no specific test procedure for the Display P.C.B. Any fault which may exist will be evident during normal operation of the Unit.

4.5 C.P.U. - P.C.B. SC 02 Circuit Diagram 959190

The C.P.U. board contains the microprocessor which controls the screen display data, control loop and receives commands from the keyboard. Part of the RAM on the board, IC30, is provided with a battery power supply to enable it to retain test set-up information.

Most of the front panel keys are connected in a matrix which connects via the Motherboard to IC22. The code corresponding to the key pressed is read from IC23 A port. A strobe signal on IC22 pin 16 generates an interrupt to initiate the response to the keystroke. The Manual Mode Level keys and Abort key are not connected to the matrix but connect to IC25 and IC24.

The front panel status indicators are driven by IC1, controlled by the data written to IC23.

The Remote Control Unit is connected to PL1. The four digit frequency display data is written to the A and B ports of IC24 and is multiplexed by IC2 andd IC3. The four outputs RO, 1, 2 and 3 define the numeral to be displayed while the outputs Digit 1, 2, 3 and 4 control which digit is illuminated.

IC4 drives a relay, IC6, which is energised (contacts closed) while the unit is driving the system amplifier, unless it is in Calibration Mode, and de-energised in all other states.

IC25 receives control signals for Start/Stop, Inhibit, Hold and Reverse functions. The Start/Stop input (PL4 pin 1) generates an interrupt on IC25 pin 18 and its level can be read on IC25 pin 4. Similarly the Inhibit and Hold inputs (PL 1 pins 14 and 21) generate an interrupt on IC25 pin 40 and the state of IC25 pins 2 and 3 is then read to identify the source of the interrupt.

C.P.U. P.C.B. SC 02 Test and Calibration

1. Connect together the rear panel NORMALISED g INPUT and SERVO OUTPUT HIGH sockets and fit a shorting plug to the SERVO OUTPUT LOW socket. Set INPUT SELECTOR switch to NORMALISED. Set the unit to run a test from 100Hz to 1000Hz at a level of 10.0g, external loop.

2. Test for continuity between pins 2 and 3 on the INTERLOCK connector. Check that there is continuity after pressing the START key and an open circuit on pressing either the STOP, ABORT or PROGRAM keys.

3. Momentarily connect together INTERLOCK pins 5 and 11 whilst the test is running and check that the test is aborted, TEST ABORTED (EXT) being displayed.

4. Connect together INTERLOCK pins 1 and 10 via a switch. With the Unit displaying READY TO START TEST open the switch and check that the test is started. Close the switch and check that the test is stopped and TEST STOPPED is displayed. Check that opening the switch continues the test.

5. Connect together INTERLOCK pins 4 and 9. Start the test. Momentarily connect together INTERLOCK pins 13 and 9 and check that the frequency sweep is reversed. Momemtarily connect together INTERLOCK pins 12 and 9 and check that the frequency sweep is stopped.

6. Start the sweep and remove the link between INTERLOCK pins 4 and 9. Check that the test is stopped, TEST STOPPED being displayed.

7. Check that the RUN and EXT LOOP status indicators are illuminated.

8. Press the CHANNEL key and check that the CH.2 status indicator is illuminated.

9. Press the PLOT key and check that the PLOT status indicator is illuminated.

10. Select Manual mode and check that the MANUAL status indicator is illuminated instead of RUN.

11. Select Program mode and check that the PROGRAM status indicator is illuminated all others being extinguished.

12. Select Run mode, internal loop and check that the RUN and INT. LOOP status indicators are illuminated.

13. Connect the Remote Control Unit to the rear panel connector and start the test. Check for correct operation of the keys, LED indicators and frequency display. (See 4.11. Remote Control Unit.)

14. Examine each of the eight tests stored in the Unit. Disconnect the Unit from the mains supply for a few minutes and then reconnect it. Check that all eight tests are stored as before. (Obviously this does not test for battery capacity, a typical unit should be able to retain test data for 5000 hours.)

4.6 Sine Generator P.C.B. SC 03 Circuit Diagram 958140 (2 Sheets).

The Sine Generator P.C.B. contains its own microprocessor and associated memory. During the power-up routine or when a new test set-up is entered the list of frequencies and sweep rate are received from the C.P.U. board via the interface comprising IC31 and IC32. The Sine Generator Board then generates the low limit frequency, FO. During a sweep the C.P.U. board receives information from the Sine Generator on current frequency, sweep count and direction. Instructions to start sweep, reverse sweep, enter Manual Mode, etc. are received by the Sine Generator in the same manner.

The frequency to be generated is specified on the output of IC5 in binary form, pin 2 is the LSB and represents 0.1Hz. The maximum frequency which can be specified by the 16 data bits is therefore 6553.5Hz. The frequency data controls the binary rate multipliers IC6, 7 and 18 to give an output clock rate, at IC19 pin 12, of 1024 times the required output frequency. IC8 provides the input clock frequency to the binary rate multiplier. The output pulses from the binary rate multiplier are counted by IC21 and IC22. This 8-bit counter addresses a PROM containing the codes required to produce the first quadrant of a sinusoidal waveform at the output of the DAC, IC39. IC37 and IC36 detect the maximum and minimum count respectively and reverse the count direction or reverse the DAC output polarity accordingly to produce the complete sinusoidal wave. The amplitude of the DAC output is set by RV1.

The 16 - bit frequency data is also used to control the tuning of the band-pass tracking filter. Analogue switches IC11 to 14 and IC24 to 27 select resistors to set the centre frequency. The value of capacitors C33 and C35 are selected to compensate for the tolerances of other filter components.

The sweep rate is controlled by timer T2 in IC4. This timer has as its input, on PB6, either a 100 microsecond clock generated by timer T1 on PB7 of IC4, or a clock of 64 times the current sine output frequency from IC21 pin 7. These are selected, for linear or logarithmic sweep respectively, by PB5 of IC4.

Sine Generator P.C.B. SC 03 Test and Calibration

1. Set the unit to generate a frequency of 400Hz. Examine the signals on TP3 and FIXED SINE OUTPUT on the oscilloscope and check that they are sensibly sinusodal and approximately 180 degrees out of phase. Change the values of C33 and C35 to adjust the phase difference if necessary. Adjust RV1 to set the signal level at FIXED SINE OUTPUT to 5.00 volts r.m.s.

2. Set the unit to generate each of the frequencies in Table 2 in turn. For each frequency, check that the output at FIXED SINE OUTPUT is sinusoidal and that its period is within the tolerance given. For frequencies greater than 20Hz check that the distortion is less than 0.1%.

Table 2. Sine Generator Frequencies

Frequency Setting	Period	
0.1 Hz	10000	+/- 10ms
0.2 Hz	5000	+/- 5ms
0.4 Hz	2500	+/- 2.5ms
0.8 Hz	1250	+/- 1.2ms
1.6 Hz	625	+/- 0.6ms
3.2 Hz	312.5	+/- 0.3ms
6.4 Hz	156.25	+/- 0.15ms
12.8 Hz	78125	+/- 78µs
25.6 Hz	39062.5	+/- 39µs
51.2 Hz	19531.3	+/- 19µs
102.4 Hz	9765.6	+/- 9.7µs
204.8 Hz	4882.8	+/- 4.8µs
409.6 Hz	2441.4	+/- 2.4µs
819.2 Hz	1220.7	+/- 1.2µs
1638.4 Hz	610.35	+/- 0.61µs
3276.8 Hz	305.18	+/- 0.31µs
6550.0 Hz	152.59	+/- 0.15µs

To change freq.
Press:
Program Key
Recall
9
Enter
Key in new Freq
Enter
RECALL
ENTER

3. Set the Unit to sweep from 1Hz to 6500Hz, open loop, output limit -99dB, at a rate of 50Hz/s. Check that the sweep time is 130s +/- 7s and that the frequency generated changes smoothly to a linear law, with stable amplitude.

4. Set the Unit to sweep from 1Hz to 6500Hz, open loop, output limit -99dB, at a rate of 5 Oct/min. Check that the sweep time is 152 +/- 8s and that the frequency generated changes smoothly to a logarithmic law, with stable amplitude.

5. With the frequency generated at approximately 5000Hz select Manual Mode. Check that pressing the frequency up and down keys in turn causes the frequency generated to increase and decrease respectively. Check that pressing the FAST key as well causes the frequency to change at a faster rate.

4.7 Compressor P.C.B. SC 04 Circuit Diagram 959200

The Sine Generator output is connected to SKT4. This signal is attenuated (compressed) in two stages which together give a range of 0 to 99.9dB attenuation with 0.1dB resolution. IC3 is connected as a low pass filter and drives the divider chain R7 to R11 which gives five 20dB attenuation steps. The required attenuation is selected by IC10, an eight - to - one multiplexer, and connected to IC14 via the buffer IC13. IC14 gives a maximum attenuation of 19.9dB with 0.1dB resolution. The digital control inputs are arranged in binary coded decimal form. It is necessary to present all three digits of new data to the attenuator simultaneously to prevent glitches at the output. This is achieved by writing the high byte (tens) into IC14 first, followed by the low byte (units and decimals) into IC42. When IC42 is written to, the first flip-flop in IC26 is also clocked. After a delay controlled by phase two of the system clock, IC26 pin 9 goes low, writing the data already set up on IC41 and IC42 outputs to IC11 and IC14 to set the new attenuation.

The attenuator output is high-pass filtered by IC27 which drives the differential servo output section comprising IC16, 28 and 48.
When internal loop operation is selected the servo output stage is disconnected by relay IC12 and the drive signal is connected to the Feedback Output, SKT 8, via IC20.

The Charge Amplifier output is connected to SKT 7, the input of the normalising amplifier, IC47. The input resistor, either R21 or R41, is selected to give the required normalised level of 10 or 100mV/g respectively. The gain of IC47 is set, according to the transducer sensitivity entered, by selecting a combination of feedback resistors with analogue switches IC17, 18, 31, 45.
The normalising amplifier output is high-pass filtered by either IC33 or IC46. IC46 has a higher roll-off frequency and is used when the lowest frequency in the test set-up is 5Hz or greater. The gain of IC19 is set by IC20 to be either 1.41 or 14.1, the higher gain being used when running a test at -20dB below the set level.

The XY plotter drive is controlled by writing data into latches IC37 and 38 (frequency) and IC39 and 40 (acceleration) to control the D-A convertors IC24 and 25. IC1 and IC2 buffer the outputs and the relay IC8 provides the pen lift control.

Compressor P.C.B. Test and Calibration

1. Remove plug from SKT 7 and connect the oscillator to SKT 7. Set INPUT SELECTOR to CHARGE. Connect DVM to NORMALISED g OUTPUT socket.

2. Enter Test Routine 0 and check gain of IC47 as given in Table 3.

Table 3. Test Routine 0.

Data At Address		Frequency and Level	Level At NORMALISED
$8DC0	$8D80	AT SC 04 SKT 7	g OUTPUT Limits
$00	$01	400 Hz, 50.0mV rms	4.750-5.250 V rms
$00	$02	400 Hz, 50.0mV rms	2.375-2.625 V rms
$00	$04	400 Hz, 50.0mV rms	1.225-1.275 V rms
$00	$08	400 Hz, 50.0mV rms	618.8-631.3mV rms
$00	$10	400 Hz, 1.00 V rms	6.188-6.313 V rms
$00	$20	400 Hz, 1.00 V rms	3.094-3.156 V rms
$00	$40	400 Hz, 1.00 V rms	1.547-1.578 V rms
$00	$80	400 Hz, 1.00 V rms	773.4-789.1mV rms
$01	$00	400 Hz, 1.00 V rms	386.7-394.5mV rms
$02	$00	400 Hz, 1.00 V rms	193.4-197.3mV rms
$00	$0A	6500 Hz, 500 mV rms	4.85 V rms minimum

3. Exit Test Routine.

4. Set up test with TRANSDUCER SENSITIVITY at 10.0pC/g and NORMALISED LEVEL at 100mV/g. Set oscillator level to 500mV at 400Hz, check DVM indication is 5.00 V r.m.s. +/-50mV.

5. Set up test with TRANSDUCER SENSITIVITY at 1.0 pC/g and NORMALISED LEVEL at 100mV/g. Set oscillator level to 50mV at 400Hz, check DVM indication is 5.00 V r.m.s. +/- 50 mV.

6. Set oscillator level to 50mV at 6.5kHz and check DVM indication is greater than 4,85 V r.m.s.

7. Disconnect oscillator, reconnect plug to SKT 7.

8. Connect short circuit on NORMALISED g input, set INPUT SELECTOR to NORMALISED, remove plug from SKT 8 and conect DVM to measure the level on SKT8 w.r.t. the screen of SKT6. Set up test to run START TEST prompt displayed adjust RV4 to null the d.c. offset indicated on the DVM.

9. Connect the oscillator to NORMALISED g INPUT. Set oscillator level to 5.00 V r.m.s. at 400Hz and adjust RV3 to obtain DVM indication of 7.07 V r.m.s.

10. Set up testr to run external loop -20dB. Set oscillator level to 500mV r.m.s. at 400Hz and check DVM indication is 6.72 to 7.42 V r.m.s.

11. Set up test heving FO. greater than 5Hz to run external loop at full lelvel. Set oscillator level to 5.00 V r.m.s. at 5Hz and check DVM indication is greater than 6.86 V r.m.s.

12. Set up test having FO. less than 5Hz to run external loop at full level. Set oscillator level to 5.00 V r.m.s. at 1Hz and check DVM indication is greater than 6.86 V r.m.s.

13. Discinnect DVM and oscillator, reconnect plug to SKT 8.

14. Connect DVM to DC ∝ f LOG/LIN. Enter Test Routine 1 and check output as given in Table 4.

Table 4. Test Routine 1.

Data at Address		Level at Rear Panel DC ∝ f LOG/LIN Limits
$8C40	$8C00	
$02	$00	5.12 V d.c. (set by RV1 SC04)
$01	$00	2.534 - 2.586 V d.c.
$00	$80	1.267 - 1.293 V d.c.
$00	$40	633.6 - 646.4 mV d.c.
$00	$20	315.0 - 325.0 mV d.c.
$00	$10	155.0 - 165.0 mV d.c.
$00	$08	75.0 - 85.0 mV d.c.
$00	$04	35.0 - 45.0 mV d.c.
$00	$02	15.0 - 25.0 mV d.c.
$00	$01	5.0 - 15.0 mV d.c.
$00	$00	-5.0 - 5.0 mV d.c.

15. Connect DVM to DC ∝ g LOG. Enter Test Routine 2 and check output as given in Table 5.

Table 5. Test Routine 2.

Data At Address		Level at Rear Panel DC ∝ g LOG Limits
$8CC0	$8C80	
$02	$00	5.12 V d.c. (set by RV2 SC04)
$01	$00	2.534 - 2.586 V d.c.
$00	$80	1.267 - 1.293 V d.c.
$00	$40	633.6 - 646.4 mV d.c.
$00	$20	315.0 - 325.0 mV d.c.
$00	$10	155.0 - 165.0 mV d.c.
$00	$08	75.0 - 85.0 mV d.c.
$00	$04	35.0 - 45.0 mV d.c.
$00	$02	15.0 - 25.0 mV d.c.
$00	$01	5.0 - 15.0 mV d.c.
$00	$00	-5.0 - 5.0 mV d.c.

16. Exit Test Routine.

17. Connect continuity meter between PLOTTER pins 14 and 15. Check that there is continuity only when unit is in control with PLOT on. Check that with PLOT off there is continuity between PLOTTER pins 13 and 14.

18. Remove plug from SKT 4 and short SKT 4. Null d.c. offset on TP1 by RV5. Null d.c. offset on TP2 by RV6. Null d.c. offset on TP4 by RV7. Reconnect plug to SKT 4.

19. Set test to generate 400Hz. Connect short circuit to SERVO OUTPUT LOW, monitor SERVO OUTPUT HIGH on oscilloscope and DVM. Select Manual mode and increase Level using slow rate. Check that output voltage changes smoothly with no glitches. Check decreasing level also. Check that output is 7.0 +/- 0.5 volts r.m.s. at 0dB.

4.8 Feedback PCB SC 05 Circuit Diagram 959210 (2 sheets)

The Feedback PCB produces an output which indicates whether the actual vibration level is above or below the required level and by how much it differs. It is supplied with the feedback signal, proportional to acceleration, from the Compressor PCB. Signals proportional to velocity and displacement are produced, by integration, at TP2 and TP4. For an acceleration signal of 10mV rms /g pk at SKT 1 the velocity signal is scaled 0.2 mV rms / mm/s pk and the displacement signal is scaled 40 mV rms / mm pk. If the 100mV/g normalised level setting is selected the voltages are all increased by a factor of ten. The two integrators IC32 and IC42 are identical. (Component references which follow apply to the first integrator.) The gain is adjusted by RV1 and feedback around IC32 is provided by C17 and a resistance selected by analogue switches IC8,9,17 and 18. Component values are arranged so that the resistance selected is approximately three times the impedance of the capacitor at the operating frequency. R38, R40 and C25 roll off the gain at low frequencies and IC43 is connected as a high-pass filter to reduce low frequency noise.

IC5,6 and 7 select either the displacement, velocity or acceleration feedback signal and set the gain of IC22 to one of four decade ranges according to the set level. IC20 is set to have a gain of between one and ten providing the fine setting of level within each decade. The combined gain of all stages is arranged to give 2V rms at TP5 when the actual level is equal to the set level. IC29 performs the rms to d.c. conversion, the d.c. output being on pin 6. IC27, 28 and associated components provide a frequency tracking time constant for smoothing the output of IC29.

The d.c. output of IC29 is compared with a 2-volt reference by IC50. The output of IC49 is high for feedback signals greater than the set level. The error magnitude is produced at the output of IC47 and is compared with eight d.c. levels by IC26 and 36 to give a digital feedback output to IC35. The feedback data is read from IC35 by the CPU board microprocessor.

Feedback PCB SC05 Test and Calibration

1. Remove C17, C75 and IC43 from the board.

2. Disconnect the plug from SKT 2 and connect the oscillator to SKT 2. Connect the DVM to TP2.

3. Enter Test Routine 3. Set oscillator output to 5.00 V r.m.s at 400Hz, adjust RV1 to obtain indication of 5.00 V r.m.s. on the DVM.

4. Check gain of IC32 as given in Table 6.

Table 6. Test Routine 3.

Data at Address		Frequency and Level at 1) SC 05 SKT2 2) SC 05 TP8	Level at 1) SC 05 TP2 2) SC 05 TP4 Limits
$8540	$8500		
$04	$00	400Hz, 5.00 V rms	5.00 V rms (set)
$00	$0A	400Hz, 50.0 mV rms	4.352 - 5.888 V rms
$00	$0B	"	3.957 - 5.353 V rms
$00	$0C	"	3.625 - 4.904 V rms
$00	$10	"	2.720 - 3.680 V rms
$00	$20	"	1.360 - 1.840 V rms
$00	$40	"	776.0 - 824.0 mV rms
$00	$80	400Hz, 500 mV rms	3.880 - 4.120 V rms
$01	$00	"	1.940 - 2.060 V rms
$02	$00	"	0.970 - 1.030 V rms
$04	$00	400Hz, 5.00 V rms	4.850 - 5.150 V rms
$08	$00	"	2.425 - 2.575 V rms
$10	$00	"	1.213 - 1.288 V rms
$20	$00	"	606.3 - 643.8 mV rms
$40	$00	"	265.6 - 359.4 mV rms
$80	$00	"	132.8 - 179.7 mV rms

5. Disconnect the oscillator from SKT2 and connect it to TP8, connect DVM to TP4. Enter Test Routine 3. Set the gain of IC42 by adjusting RV2 and check gain as given in Table 6.

6. Disconnect the oscillator from TP8. Replace C17, C75 and IC43. Connect the oscillator to SKT2 and the DVM to TP2.

7. Enter Test Routine 4. Set oscillator output to 5.00V r.m.s. at 31.6Hz. Adjust RV1 to obtain level of 5.00V r.m.s. at TP2. Connect DVM to TP4 and adjust RV2 to obtain level of 5.00V r.m.s. at TP4.

8. Connect the DVM to TP1 and check the gain of IC22 as given in Table 7.

Table 7. Test Routine 4.

Data at Address $8580	Frequency and Level at SC 05 SKT2	Level at SC 05 TP1 Limits
$0C	31.6Hz 2.50V rms	495.0 - 505.0mV rms
$18	31.6Hz 2.50V rms	4.950 - 5.050 V rms
$28	31.6Hz 250 mV rms	4.950 - 5.050 V rms
$48	31.6Hz 25.0mV rms	4.950 - 5.050 V rms
$06	31.6Hz 5.00V rms	4.950 - 5.050 V rms
$12	31.6Hz 500mV rms	4.950 - 5.050 V rms
$22	31.6Hz 50.0mV rms	4.950 - 5.050 V rms
$42	31.6Hz 5.00mV rms	4.950 - 5.050 V rms
$05	31.6Hz 1.00V rms	495.0 - 505.0mV rms
$11	31.6Hz 1.00V rms	4.950 - 5.050 V rms
$21	31.6Hz 100mV rms	4.950 - 5.050 V rms
$41	31.6Hz 10.0mV rms	4.950 - 5.050 V rms

9. Enter Test Routine 5. Connect the DVM to TP5 and set the oscillator level to give a DVM indication of 5.00V r.m.s. Check the level at TP5 for data values given in the first four lines of Table 8. For the remaining steps in Table 8 set the oscillator to obtain the level specified at TP1 and check the resulting level at TP5.

Table 8. Test Routine 5.

Data at Address $8440	Data at Address $8400	Frequency and Level at SC 05 TP1	Level at SC 05 TP5 Limits
$00	$01	400Hz (5.0mV)	5.00 V rms (set)
$00	$02	400Hz (5.0mV)	2.38 - 2.63 V rms
$00	$04	400Hz (5.0mV)	1.19 - 1.31 V rms
$00	$08	400Hz (5.0mV)	0.594 - 0.656V rms
$00	$08	400Hz 50.0mV rms	5.94 - 6.56 V rms
$00	$10	400Hz 50.0mV rms	3.094 - 3.156V rms
$00	$20	400Hz 50.0mV rms	1.547 - 1.578V rms
$00	$40	400Hz 50.0mV rms	773.4 - 789.1mV rms
$00	$80	400Hz 500mV rms	3.867 - 3.945V rms
$01	$00	400Hz 500mV rms	1.934 - 1.973V rms
$02	$00	400Hz 500mV rms	966.8 - 986.3mV rms

10. Enter Test Routine 6. Set oscillator output to give a level of 2.00V r.m.s. at 400Hz at TP5. Check that the level at TP7 is 1.98 to 2.02V d.c.

11. For each entry in Table 9 set oscillator output to give a level of 2.00V r.m.s. at TP5 at the frequency specified. Monitor TP7 on the oscilloscope and DVM and check mean level is 2.0V d.c. with between 20 and 40mV peak to peak ripple.

Table 9. Test Routine 6.

Data at Address $8480	Data at Address $84C0	Frequency and Level at SC 05 TP5	Level at SC 05 TP7
$00	$00	400Hz 2.00V rms	1.98 - 2.02V d.c.
$00	$00	1.6Hz 2.00V rms	2.0V d.c. mean with 20-40mV p-p ripple
$00	$20	4.8Hz 2.00V rms	" "
$00	$40	8.0Hz 2.00V rms	" "
$00	$80	14.4Hz 2.00V rms	" "
$01	$00	25.6Hz 2.00V rms	" "
$02	$00	51.2Hz 2.00V rms	" "
$04	$00	102Hz 2.00V rms	" "
$08	$00	205Hz 2.00V rms	" "
$10	$00	410Hz 2.00V rms	" "
$20	$00	820Hz 2.00V rms	" "
$40	$00	1640Hz 2.00V rms	" "
$80	$00	3280Hz 2.00V rms	" "

12. Enter Test Routine 6 and advance through to obtain a data display of $10 $00. Set the oscillator output to 400Hz at a level to give 2.00V r.m.s. at TP5. Monitor TP6 on the oscilloscope and adjust RV3 to obtain a square wave on TP6 with equal mark-space ratio.

13. Monitor IC35 pin 2 on the oscilloscope and check that it is at a logic low level (less than 0.8V), if it is high, turn RV4 anticlockwise until it goes low.

14. Increase the oscillator level to the point where IC35 pin 2 begins to switch to a logic high and note the signal level on TP5. (Reading A, typically 2.02V r.m.s.). Decrease the oscillator level and locate the other point where IC35 pin 2 begins to switch to a logic high and note the signal level on TP5. (Reading B, typically 1.98V r.m.s.).

15. Subtract reading B from reading A and adjust RV4 to produce a result of 0.04V r.m.s. (Turn RV4 clockwise to decrease the difference between A and B).

16. Set the switching points, readings A and B, symetrically about 2.00V r.m.s. by adjusting RV3. (Turn RV3 clockwise to decrease the readings obtained at the switching points). The switching points for pin 2 should now be 1.98 and 2.02V r.m.s.

17. Monitor each pin of IC35 listed in Table 10. Check that the level on each pin is low (less than 0.8V) whilst the level in TP5 is within the range specified, and high (greater than 2.4V) whilst outside the range specified. (Figures given are typical.)

Table 10. Feedback Data Output

Error Bit	IC35 Pin	Low Switching Volts r.m.s.	High Switching Volts r.m.s.
0	2	1.98	2.02
1	3	1.95	2.05
2	4	1.90	2.10
3	5	1.78	2.22
4	6	1.55	2.45
5	7	1.26	2.8
6	8	0.57	3.3
7	9	-	5.9

18. Disconnect the oscillator from SKT2 and replace plug in SKT2.

4.9 Metering P.C.B. SC 06 Circuit Diagram 958170 (2 Sheets)

The metering P.C.B. is very similar in some areas to the Feedback P.C.B. Only sections which are different will be described.

Channel 2 metering input from the rear panel is amplified by IC45, its gain being set by RV5 to the square root of two. Channel 1/ Channel 2 switching is performed by IC9, controlled by IC35.

The displacement, velocity and acceleration signals are selected by IC6, 7 and 22. The gain of IC20 and IC43 is controlled by the data written to IC36.

The output of IC3, the r.m.s. to d.c. convertor, is connected to the DVM chip, IC1. This is set up by RV1 (zero) and RV2 (full scale). A to D convertion is initiated by a pulse on IC29 pin 39. The DVM data output is read from IC29 A and B ports by the CPU board microprocessor. The data is tested to determine whether a range change is required.

Metering P.C.B. SC 06 Test and Calibration.

1. Remove C29, C38 and IC11 from the board.

2. Disconnect the plug from SKT1 and connect the oscillator to SKT1. Connect the DVM to TP3.

3. Enter Test Routine 7. Set oscillator output to 5.00V r.m.s. at 400Hz, adjust RV3 to obtain indication of 5.00V r.m.s. on the DVM.

4. Check gain of IC10 as given in Table 11.

Table 11. Test Routine 7.

Data at Address $8940	Data at Address $8900	Frequency and level at 1) SC 06 SKT1 2) SC 06 TP5	Level at 1) SC 06 TP3 2) SC 06 TP4 Limits
$04	$00	400Hz 5.00 V rms	5.00 V rms (set)
$00	$0A	400Hz 50.0mV rms	4.352 - 5.888 V rms
$00	$0B	400Hz 50.0mV rms	3.957 - 5.353 V rms
$00	$0C	400Hz 50.0mV rms	3.625 - 4.904 V rms
$00	$10	400Hz 50.0mV rms	2.720 - 3.680 V rms
$00	$20	400Hz 50.0mV rms	1.360 - 1.840 V rms
$00	$40	400Hz 50.0mV rms	776.0 - 824.0mV rms
$00	$80	400Hz 500 mV rms	3.880 - 4.120 V rms
$01	$00	400Hz 500 mV rms	1.940 - 2.060 V rms
$02	$00	400Hz 500 mV rms	0.970 - 1.030 V rms
$04	$00	400Hz 5.00 V rms	4.850 - 5.150 V rms
$08	$00	400Hz 5.00 V rms	2.425 - 2.575 V rms
$10	$00	400Hz 5.00 V rms	1.213 - 1.288 V rms
$20	$00	400Hz 5.00 V rms	606.3 - 643.8mV rms
$40	$00	400Hz 5.00 V rms	265.6 - 359.4mV rms
$80	$00	400Hz 5.00 V rms	132.8 - 179.7mV rms

5. Disconnect the oscillator from SKT1 and connect it to TP5, connect the DVM to TP4. Enter Test Routine 7. Set the gain of IC12 by adjusting RV4 and check gain as given in Table 11.

6. Disconnect the oscillator from TP5. Replace C29, C38 and IC11. Connect the oscillator to SKT1 and the DVM to TP3.

7. Enter Test Routine 8. Set oscillator output to 5.00V r.m.s. at 31.6Hz. Adjust RV3 to obtain level of 5.00 V r.m.s. at TP3. Connect DVM to TP4 and adjust RV4 to obtain level of 5.00 V r.m.s. at TP4.

8. Connect the DVM to TP6 and check the gain of IC20 and IC43 as given in Table 12.

Table 12. Test Routine 8.

Data at Address $8980	Frequency and Level at SC 06 SKT1	Level at SC 06 TP6 Limits
$0C	31.6Hz 5.00 V rms	495.0 - 505.0mV rms
$18	31.6Hz 5.00 V rms	4.950 - 5.050 V rms
$28	31.6Hz 500 mV rms	4.950 - 5.050 V rms
$A8	31.6Hz 50.0mV rms	4.950 - 5.050 V rms
$06	31.6Hz 1.00 V rms	495.0 - 505.0mV rms
$12	31.6Hz 1.00 V rms	4.950 - 5.050 V rms
$22	31.6Hz 100 mV rms	4.950 - 5.050 V rms
$A2	31.6Hz 10.0mV rms	4.950 - 5.050 V rms
$05	31.6Hz 2.00 V rms	495.0 - 505.0mV rms
$11	31.6Hz 2.00 V rms	4.950 - 5.050 V rms
$21	31.6Hz 200 mV rms	4.950 - 5.050 V rms
$A1	31.6Hz 20.0mV rms	4.950 - 5.050 V rms

9. Enter Test Routine 9. Set oscillator output to give a level of 2.00V r.m.s. at 400Hz at TP6. Check that the level on TP1 is 1.98 to 2.02V d.c.

10. For each entry in Table 13, set oscillator output to give a level of 2.00V r.m.s. at TP6 at the frequency specified. Monitor TP1 on the oscilloscope and DVM and check mean level is 2.0V d.c. with between 5 and 15mV peak to peak ripple.

Table 13. Test Routine 9.

Data at Address		Frequency and Level at SC 06 TP6		Level at SC 06 TP1
$8880	$88C0			
$00	$00	400Hz	2.00 V rms	1.98 - 2.02 V d.c.
$00	$00	1.6Hz	2.00 V rms	2.0 V d.c. mean with 5 - 15mV p-p ripple
$00	$20	4.8Hz	2.00 V rms	" "
$00	$40	8.0Hz	2.00 V rms	" "
$00	$80	14.4Hz	2.00 V rms	" "
$01	$00	25.6Hz	2.00 V rms	" "
$02	$00	51.2Hz	2.00 V rms	" "
$04	$00	102Hz	2.00 V rms	" "
$08	$00	205Hz	2.00 V rms	" "
$10	$00	410Hz	2.00 V rms	" "
$20	$00	820Hz	2.00 V rms	" "
$40	$00	1640Hz	2.00 V rms	" "
$80	$00	3280Hz	2.00 V rms	" "

11. Exit from Test Routine. Select Program mode, set the Normalised Level to 100mV/g and then select the Transducer Calibration mode.

12. Set oscillator output to 100mV r.m.s. at 400Hz and adjust RV1 to obtain an indication of 1.00g on the DSC8.

13. Set oscillator output to 1.900 V r.m.s. and adjust RV2 to obtain an indication of 19.00g on the DSC 8.

14. Repeat the previous two paragraphs until no further adjustment of RV1 and RV2 is necessary.

15. Disconnect the oscillator from SKT1 and re-connect the plug to SKT1. Connect the oscillator to CH.2 NORMALISED INPUT and set its output to 5.00 V r.m.s. at 400Hz. Adjust RV5 to obtain a level of 7.07V r.m.s. at the output of IC45.

4.10 Charge Amplifier P.C.B. SC 10 Circuit Diagram 958610

Integrated circuit IC1 operates as a charge amplifier due to feedback through C1. Resistors R2, R3 and R4 provide d.c. stabilisation and, with C1, set the low frequency roll-off. Resistor R1 and the effective capacitance of the accelerometer determine the high frequency roll-off.

The input connector screen is connected to the rear panel and screening box in which the P.C.B. is fitted. Integrated circuit IC3 is used to reference the output to the OV line of the Unit.

Charge Amplifier SC 10 Test and Calibration.

In the following procedure it is assumed that the normalising amplifier on the Compressor P.C.B. is operating correctly.

1. Set the INPUT SELECTOR to NORMALISED, set the TRANSDUCER SENSITIVITY to 10.0 pC/g and the NORMALISED LEVEL to 10mV/g. Connect the oscillator to the CHARGE INPUT microdot socket via a 10nF capacitor using low noise cable. Monitor the NORMALISED g OUTPUT on the oscilloscope. Set the oscillator output to 400Hz and increase the level until the NORMALISED g OUTPUT begins to clip. Check that this does not occur until the signal is greater than 10 volts peak. Adjust RV1 if necessary to achieve this.

2. Replace the 10nF capacitor by a 1nF capacitor. Set the oscillator output to 5.000V r.m.s. at 400Hz and check that the NORMALISED g OUTPUT is 4.925 to 5.075V r.m.s.

3. Set the oscillator output to 5.00V r.m.s. at 6.5kHz and check that the NORMALISED g OUTPUT is 4.85 to 5.15V r.m.s.

4. Repeat the previous paragraph at a frequency of 1Hz.

4.11 GPIB Interface SC11 & SC12 Circuit Diagram 959230

All control of interface states and data transfer is controlled by IC4. This device is interfaced to the 6502 bus by IC1 and IC2.

The rear panel ADDRESS and FUNCTION switches are connected via flat strip cable to IC3. The switches are closed when set to the 1 position, as indicated on the rear panel, pulling the inputs to IC3 low. The data read from IC3 is inverted by the software to convert it back to positive logic. The link on IC3 between pins 15 and 19 is used by the power-on reset routine to test whether or not the GPIB is fitted to the unit.

GPIB Interface Test and Calibration

A fault in the interface will be evident during normal operation of the unit. The example programs given in the Instruction Manual may be used to test the interface.

4.12 Remote Control Unit Circuit Diagram 958660

The keys on the Remote Control Unit are connected in parallel with the five Run mode keys on the DSC 8 to duplicate their functions.

The frequency display is controlled by IC1. The four lines DIGIT 1, 2, 3 and 4 address each digit in turn to de-multiplex the frequency information.

Remote Control Unit - Test And Calibration

1. Connect the R.C.U. to the DSC 8.
   Set up the DSC 8 to perform a sweep test from 5Hz to 6000Hz at 10g, internal loop.

2. Start the test, check that all LED indicators except the sweep up are extinguished, check that the R.C.U. frequency display agrees with that on the DSC 8.

3. Test the operation of the R.C.U. HOLD and STOP keys in turn. As each is pressed the integral LED should light. Press the START key to continue the test.

4. Test the operation of the R.C.U. REV key. Check that the illumination of the sweep direction arrows is changed each time the key is pressed.

5. Test the operation of the R.C.U. ABORT key. Check that the integral LED is illuminated and that TEST ABORTED (OPR) is displayed on the DSC 8.

4.13 C.R.T. Display Drive Board

The following pre-set controls are provided on the C.R.T. display drive board, type DDF5C.

Contrast	RV1
Line Hold	RV2
Brilliance	RV3
Phase	RV4
Focus	RV5
Frame Linearity	RV6
Height	RV7
Frame Hold	RV8
Width	L2

The deflection coil assembly on the tube neck is fitted with magnets which affect the display position and correct the display shape.

4.14 Fault Finding Information

Of the types of faults likely to occur, those in the analogue sections of a board are relatively straight-forward to locate. Faults in the digital sections divide into two groups: a) those which only affect the operation of the board on which they occur, and b) those which affect the operation of the whole Unit. If a fault in the second group occurs it may be difficult to identify the faulty board. The following information is intended to assist with this condition.

4.14.1 Power-up Sequence

SC 02 IC21 pin 2 is low for approximately 100 ms after the +5V supply is established, providing the system reset control. The rising edge of the RES line starts program execution, initialising various sections of the unit. The sequence is given below.

1. Initialise CRT Controller SC 01 IC21.
   Set up number of lines per page etc. No response is required from SC 01.

2. Light PROGRAM LED.
   (Until this is done all seven LEDs will be illuminated)

3. Blank display.
   Write spaces to all screen locations. $\overline{\text{Vsync}}$ must be received from SC 01 before writing is performed.

4. Display Menu page.
(Also timed by Vsync)

5. Send test frequency data to Sine Generator.
Transfer of frequency and sweep data under handshake control to SC 03.

6. Display Metering page.(Also timed by Vsync).
Light RUN and EXT LOOP LEDs.

7. Await keyboard input.

4.14.2 Operation with Plug-in Boards Removed.

In order to locate faults on the Motherboard side of the bus buffers it may be necessary to operate the unit with some of the plug-in boards removed. Recommended combinations of boards together with details of the extent to which the Unit will operate, assuming that those boards which are fitted are in working condition, are given below.

It must be remembered that satisfactory limited operation of one of the combinations of boards given does not ensure that these boards are fully operational. It is only the non-functioning of a particular set of boards which shows that one of that set is faulty.

Note that the OV rail is connected to ground via the display board SC 01. When this board is removed an alternative connexion should be made between the OV rail (pins 3 & 5 on the Motherboard) and chassis.

Board fitted: SC 02
Power-up: PROGRAM LED on.
Operation: No response to keyboard. IRQ (IC25 pin 21) remains high at all times.

Board fitted: SC 03
Power-up: Sine output unpredictable.
Operation: Momentarily short RES IC34 pin 11 to OV.
Sine output 6500 Hz whilst RES is low, changes to 100 Hz after RES goes high.

Boards fitted: SC 01, SC 02
Power-up: PROGRAM LED on, Menu page displayed.
Operation: Pressing any key causes IRQ to go low and remain low. No other response.

Boards fitted: SC 01, SC 02, SC 03
Power-up: RUN and EXT LOOP LEDs on, Metering page displayed.
Sine generator output = low limit frequency, FO.
Operation: Pressing ABORT key causes TEST ABORTED (INT) to be displayed, IRQ remaining low afterwards. Pressing any key other than ABORT causes TEST ABORTED (INT) to be displayed, IRQ returns high after first pressing, but remains low after second pressing.

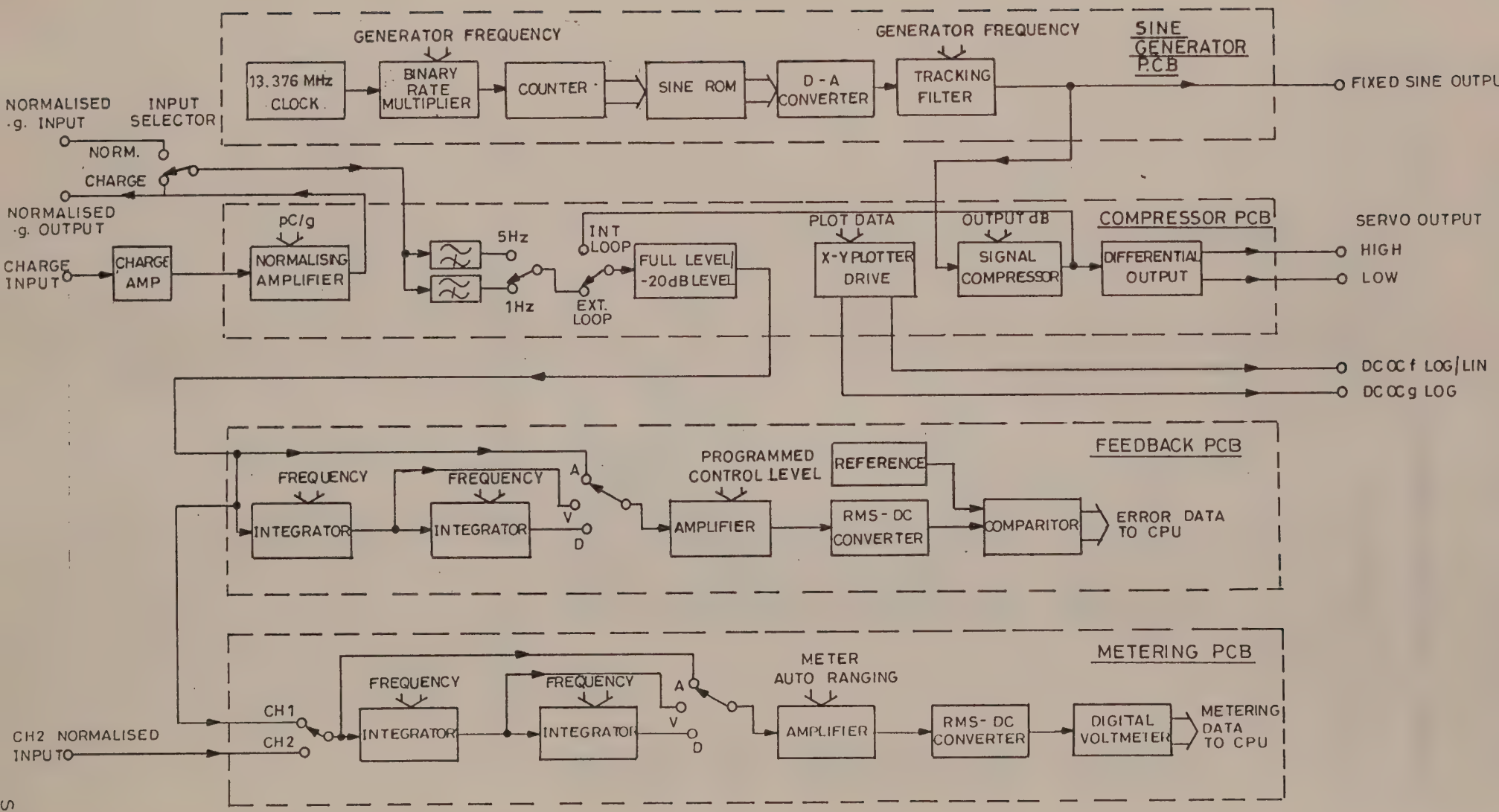
Boards fitted: SC 01, SC 02, SC 03, SC 04.
Power-up: As above.
Operation: Moving INPUT SELECTOR switch causes TEST ABORTED (INT) to be displayed. IRQ returning high afterwards. Pressing any key causes IRQ to remain low, no other response.

Boards fitted: SC 01, SC 02, SC 03, SC 04, SC 05
Power-up: As above.
Operation: Moving INPUT SELECTOR sswich causes TEST ABORTED (INT) to be displayed, IRQ returning high afterwards.
START key starts test, TEST STARTED, TEST IN PROGRESS being displayed, frequency sweeps, no display update of frequency, level, sweep count on CRT.
Pressing ABORT causes shutdown, START key will not restart test.
Operation of $\overline{IRQ}$ normal.

SECTION 5 - RECOMMENDED SPARES LIST

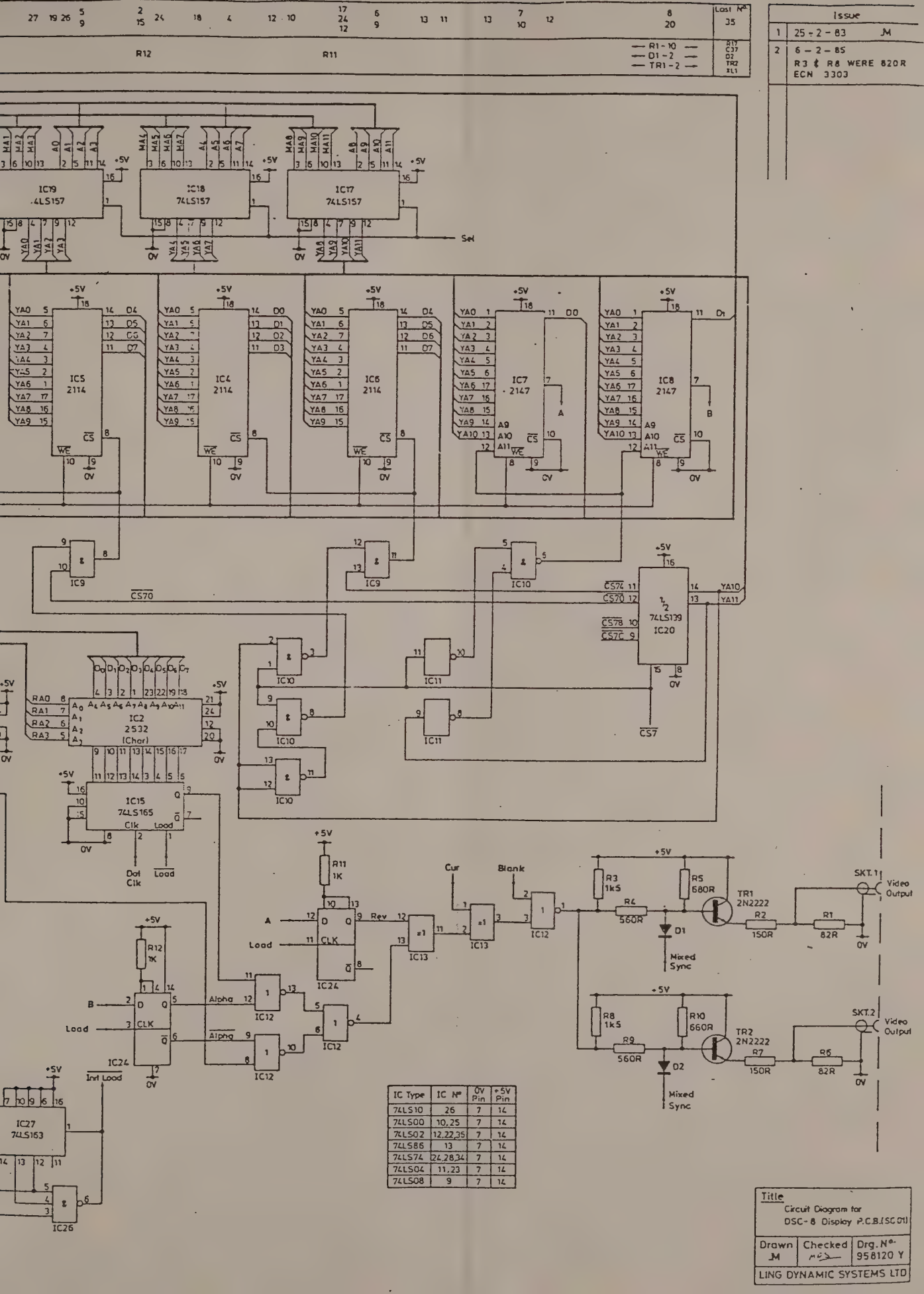
Part No.	Description	First Line Repair (1)	Spares Kit Incl. 1 & 2 (2)
779000	PCB Display CRT		1
779470	PCB CPU		1
779020	PCB Sine Generator		1
779480	PCB Compressor		1
779490	PCB Feedback		1
779050	PCB Metering		1
779080	PCB Extension		1
794950	GPIB Interface		1*
779070	PCB Status		1
654940	Power Supply		1
654960	CRT Type G23-125GH		1
654970	CRT Drive Assy		1
526600	Keyboard		1
526620	Screw Status Panel		1
342110	Thumbwheel	1	
665880	POT IK	1	
665890	POT 100 K	1	
747450	Flatstrip	1	
833840	Keyswitch AML27 ABK 2AC02AA	1	
708810	Fuse 2A	2	
867950	7 Segment Display Type. 5082-7651 (RCU)	1	
867960	LED (RCU)	1	
862510	IC LF 356H (Charge Amp)	1	
863290	IC LF 356N (Charge Amp)	1	
863790	IC 74LS47 (RCU)	1	
832700	Switch SW2, 3 (RCU)	1	
832710	Switch SW1,4,5 (RCU)	1	

* Required for Units fitted with GPIB Interface option only.


GENERATOR FREQUENCY
13.376 MHz CLOCK
BINARY RATE MULTIPLIER
COUNTER
SINE ROM
D-A CONVERTER
GENERATOR FREQUENCY
TRACKING FILTER
SINE GENERATOR P.C.B
FIXED SINE OUTPUT
NORMALISED g. INPUT
INPUT SELECTOR
NORM.
CHARGE
NORMALISED g. OUTPUT
CHARGE INPUT
CHARGE AMP
pC/g
NORMALISING AMPLIFIER
5Hz
1Hz
INT LOOP
EXT. LOOP
FULL LEVEL/ -20dB LEVEL
PLOT DATA
X-Y PLOTTER DRIVE
OUTPUT dB
SIGNAL COMPRESSOR
COMPRESSOR PCB
DIFFERENTIAL OUTPUT
SERVO OUTPUT
HIGH
LOW
DC OC f LOG/LIN
DC OC g LOG
FEEDBACK PCB
FREQUENCY
INTEGRATOR
FREQUENCY
INTEGRATOR
A
V
D
PROGRAMMED CONTROL LEVEL
AMPLIFIER
REFERENCE
RMS-DC CONVERTER
COMPARITOR
ERROR DATA TO CPU
METERING PCB
FREQUENCY
INTEGRATOR
FREQUENCY
INTEGRATOR
A
V
D
METER AUTO RANGING
AMPLIFIER
RMS-DC CONVERTER
DIGITAL VOLTMETER
METERING DATA TO CPU
CH1
CH2
CH2 NORMALISED INPUT

SHEET

| | | |

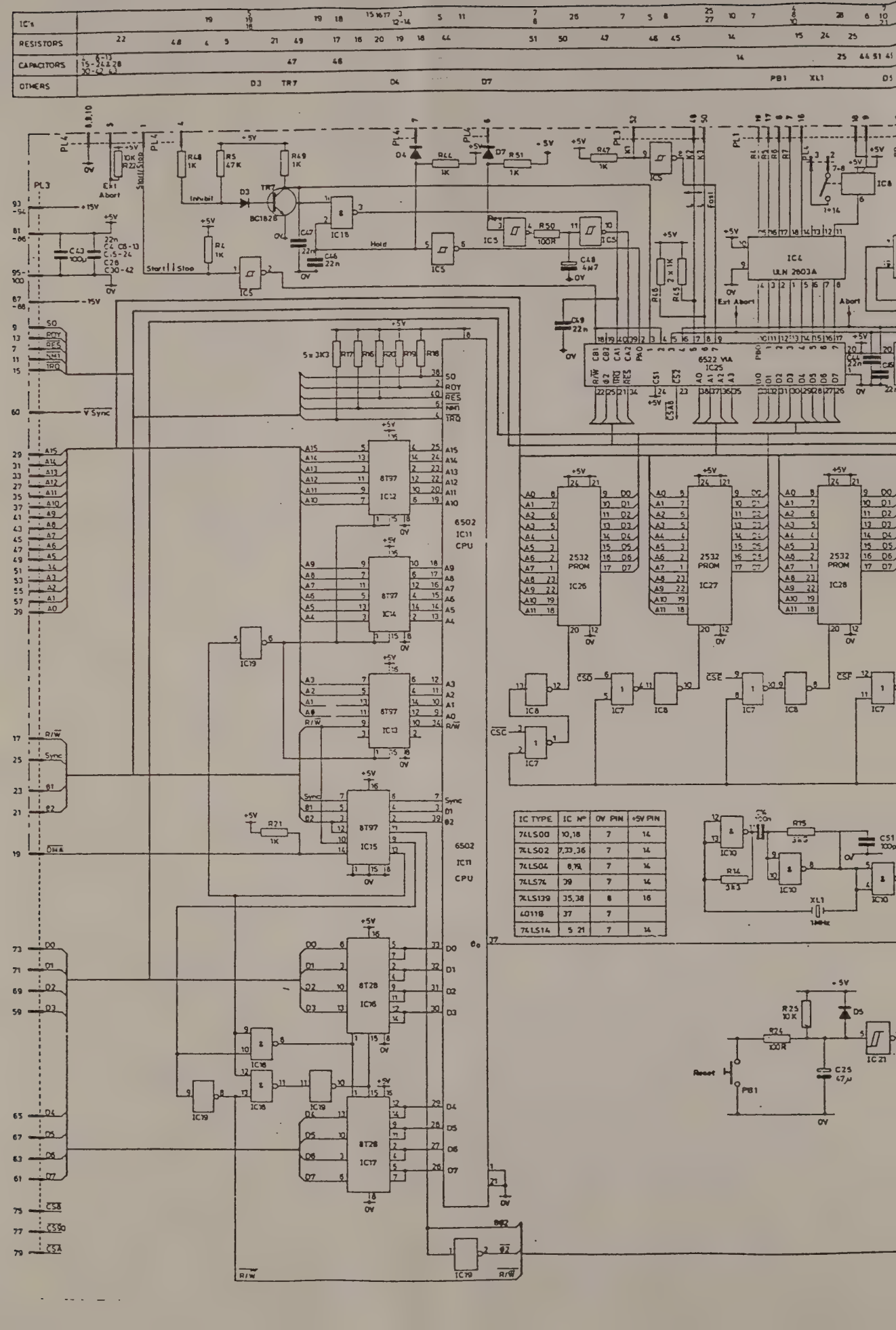


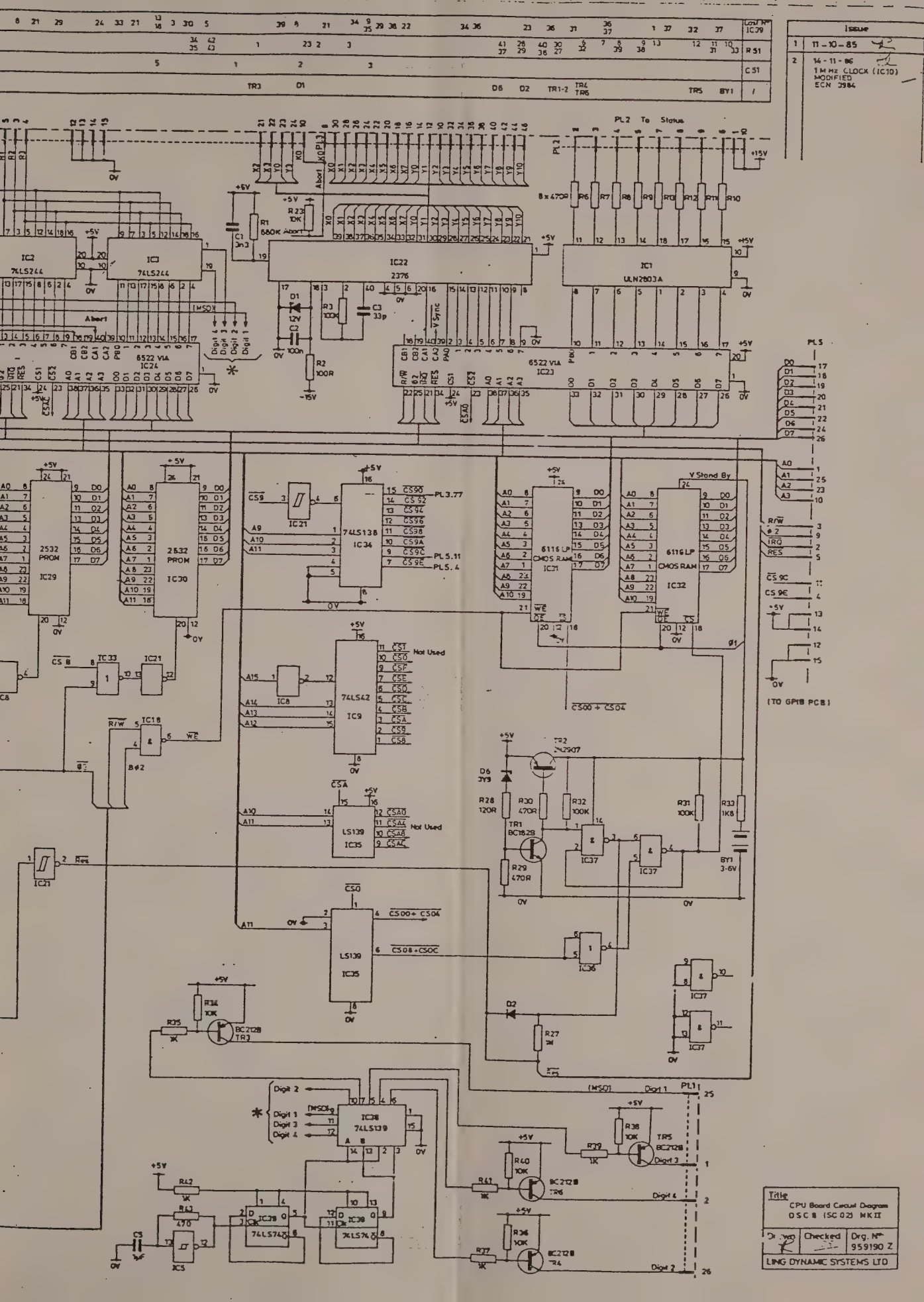
IC Type	IC No	0V Pin	+5V Pin
74LS10	26	7	14
74LS00	10,25	7	14
74LS02	12,22,35	7	14
74LS86	13	7	14
74LS74	24,28,34	7	14
74LS04	11,23	7	14
74LS08	9	7	14

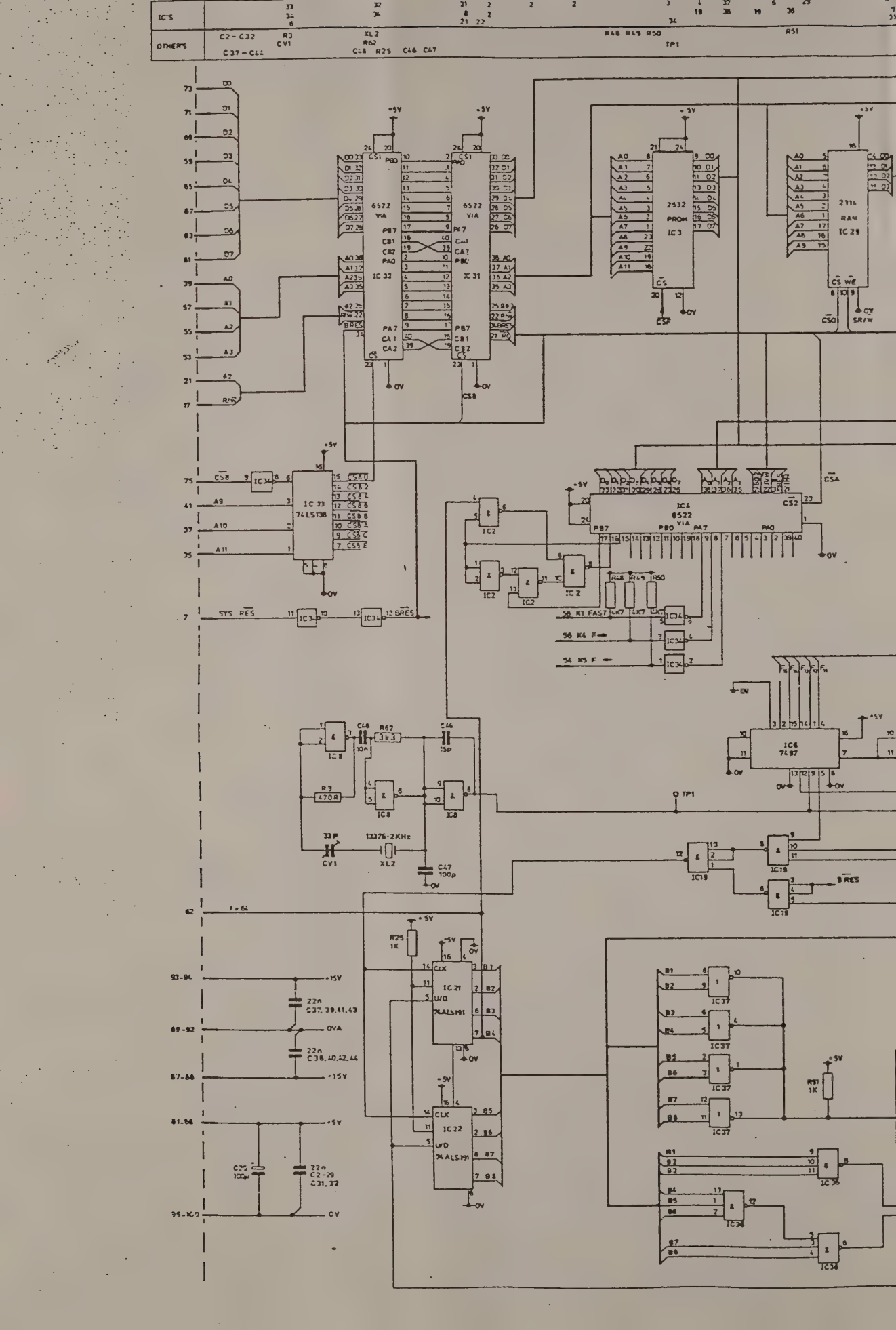
Title
Circuit Diagram for
DSC-8 Display P.C.B. (SC011)

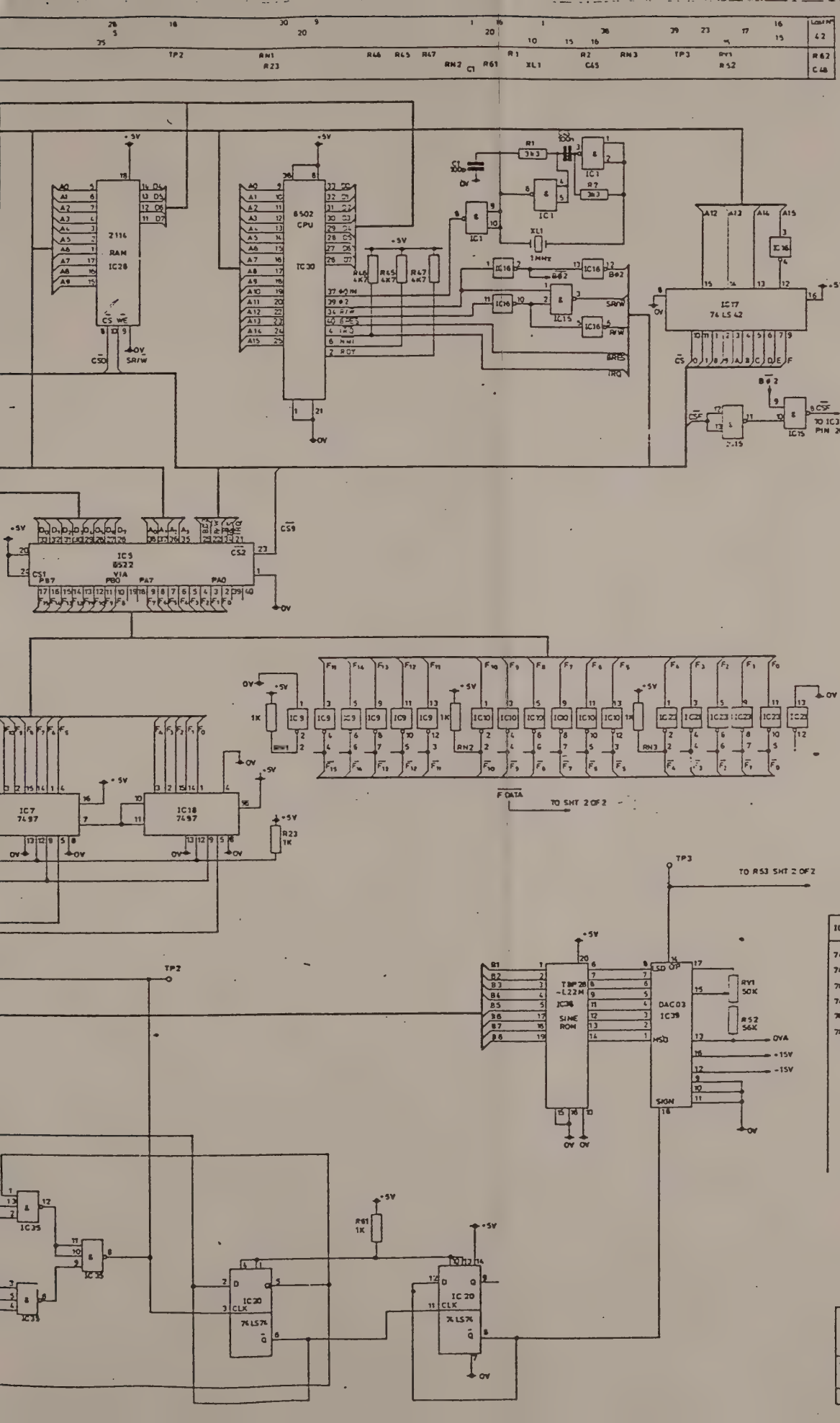
Drawn	Checked	Drg. No.
JM		958120 Y

LING DYNAMIC SYSTEMS LTD


IC's
RESISTORS
CAPACITORS
OTHERS
+5V
0V
6502 CPU
6522 VIA
2532 PROM
ULN 2803A
8T97
8T28
Start / Stop
Abort
Reset
Hold
Inhibit
Ext Abort
V Sync
R/W
Sync
CSA
CSB
CSC
CSD
CSE
CSF
1MHz
IC TYPE | IC Nº | 0V PIN | +5V PIN
74LS00 | 10,18 | 7 | 14
74LS02 | 7,33,36 | 7 | 14
74LS04 | 8,92 | 7 | 14
74LS74 | 39 | 7 | 14
74LS139 | 35,38 | 8 | 16
40118 | 37 | 7 |
74LS14 | 5 21 | 7 | 14


Issue
1 11-10-85
2 14-11-86
1 MHz CLOCK (IC10) MODIFIED ECN 3984
PL2 To Status
IC2 74LS244
IC3 74LS244
IC22 2376
IC1 ULN2803A
IC24 6522 VIA
IC23 6522 VIA
IC29 2532 PROM
IC30 2532 PROM
IC31 6116 LP CMOS RAM
IC32 6116 LP CMOS RAM
IC34 74LS138
IC9 74LS42
IC35 LS139
IC38 74LS139
IC39 74LS74
IC40 74LS74
IC18
IC21
IC33
IC8
IC37
IC36
IC5
TR1 BC182B
TR2 2N2907
TR3 BC212B
TR4 BC212B
TR5 BC212B
TR6 BC212B
BT1 3·6V
PL1
PL5
(TO GPIB PCB)
Title
CPU Board Circuit Diagram
OSCB (SC02) MKII
Drawn
Checked
Drg. No 959190 Z
LING DYNAMIC SYSTEMS LTD

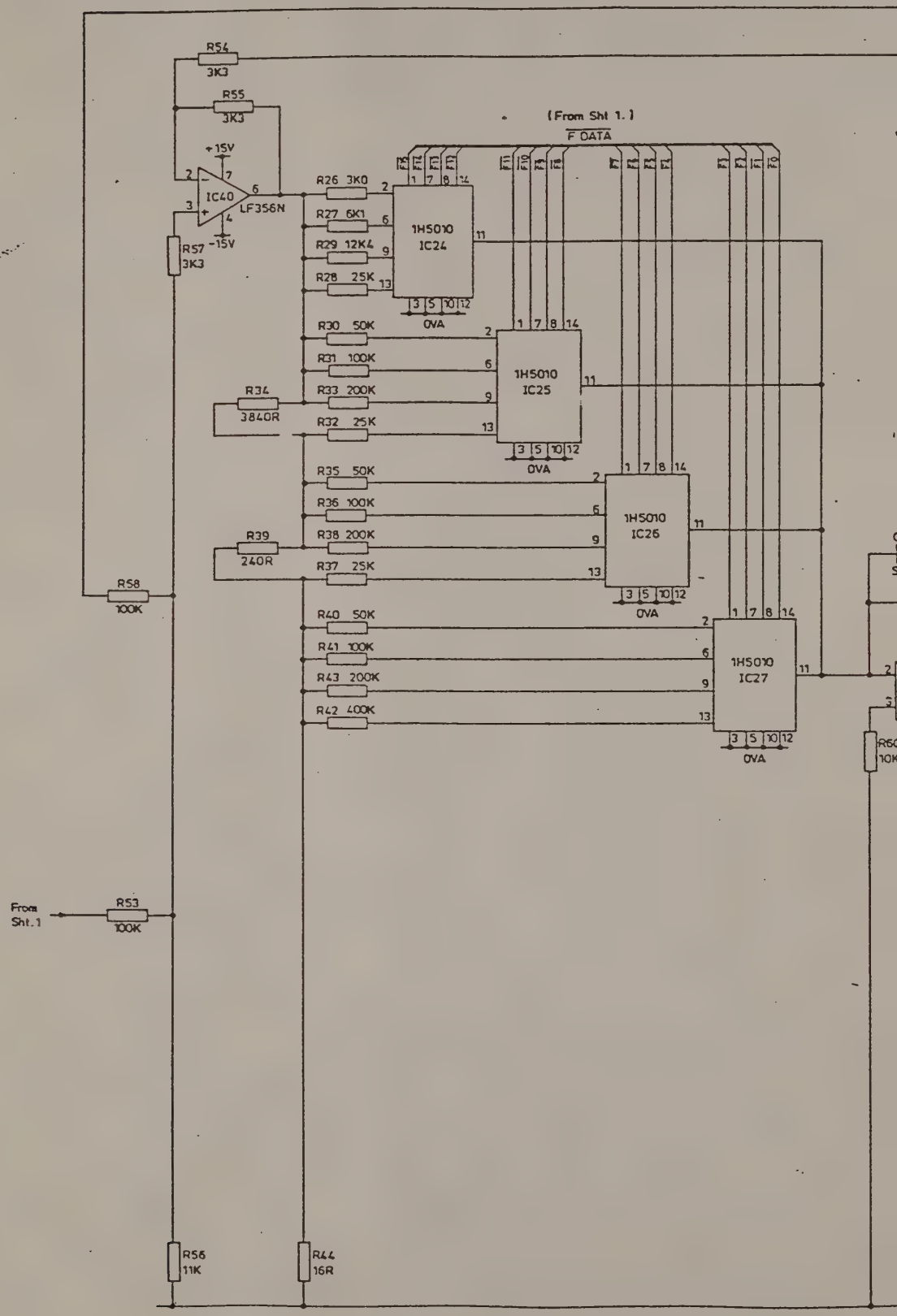

IC'S
OTHER'S
C2 - C32
C37 - C44
R3
CV1
XL2
R62
C48 R25 C46 C47
R48 R49 R50
R51
TP1
6522 VIA
IC 32
IC 31
2532 PROM
IC3
2114 RAM
IC 29
74LS138
IC 33
8522 VIA
IC4
7497
IC6
74ALS191
IC 21
IC 22
13376-2KHz
470R
3k3
100n
15P
33P
100µ
1K
+5V
0V
-15V
+15V
0VA
SYS RES
BRES
CS0
CS1
CS2
CS3
CS4
CS5
CS6
CS7
CS8
R/W
SRW



IC TYPE	IC Nº	0V PIN	5V PIN
74 LS 00	1, 2, 8, 15,	7	14
74 LS 04	16 , 34,	7	14
74 LS 05	9, 10, 23,	7	14
74 LS 10	19 , 35,	7	14
74 LS 11	36	7	14
74 LS 32	37	7	14

Title	Circuit Diagram Sine Generator P.C.B DSC-8 (SC03) Sht 1 Of 2	
Drawn	Checked	Drg. N°. 958140 Z
LING DYNAMIC SYSTEMS LTD		

ICs	40	24	25	26	27
CAPACITORS					



4-22					59		Last N° 62
	11	12	13	14	42		42
4					35	36	44

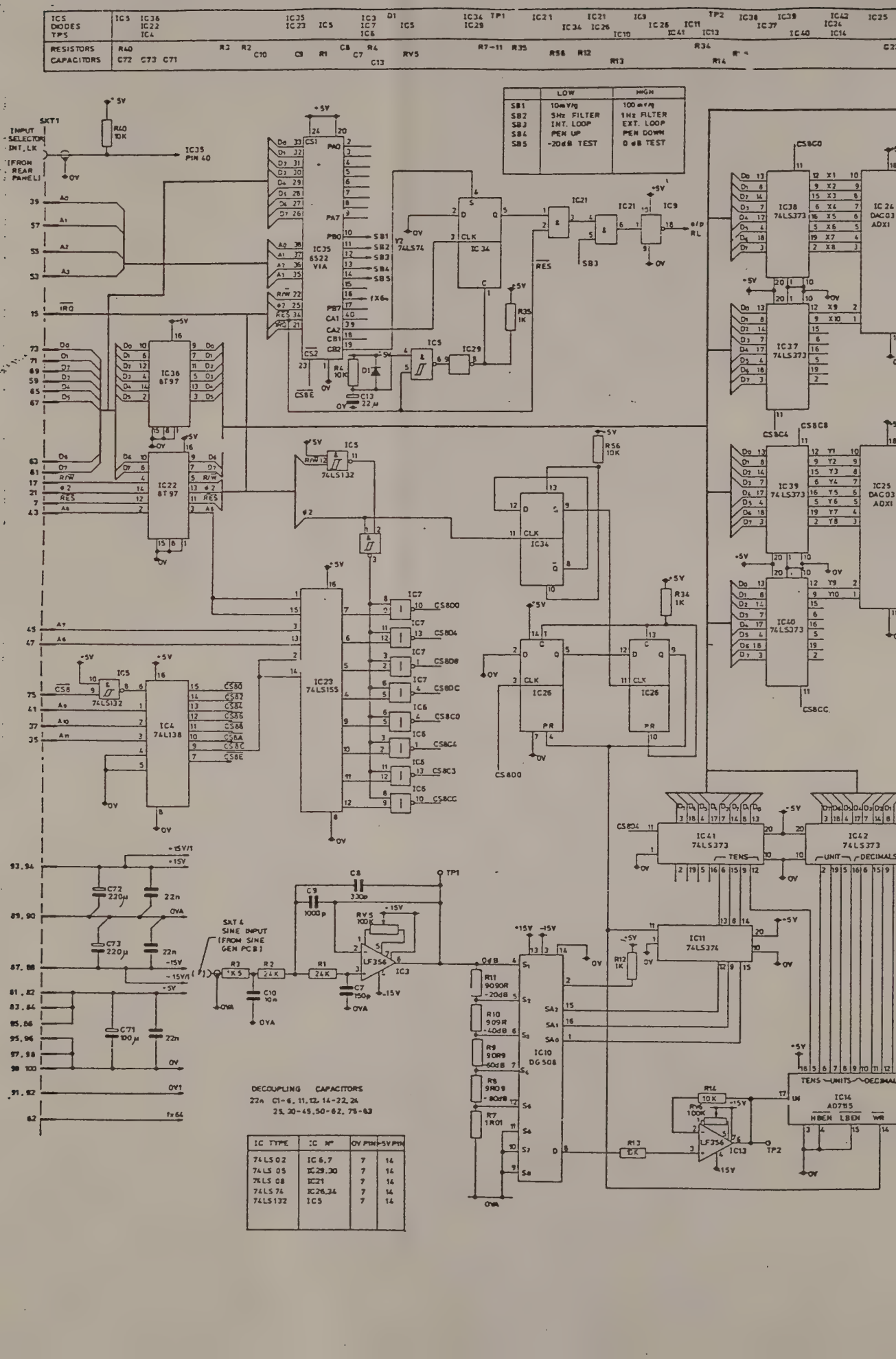
Issue		
1	25-7-83	JM
2	6-2-85 SEE SHT 1	
3	14-11-86 SEE SHT 1.	

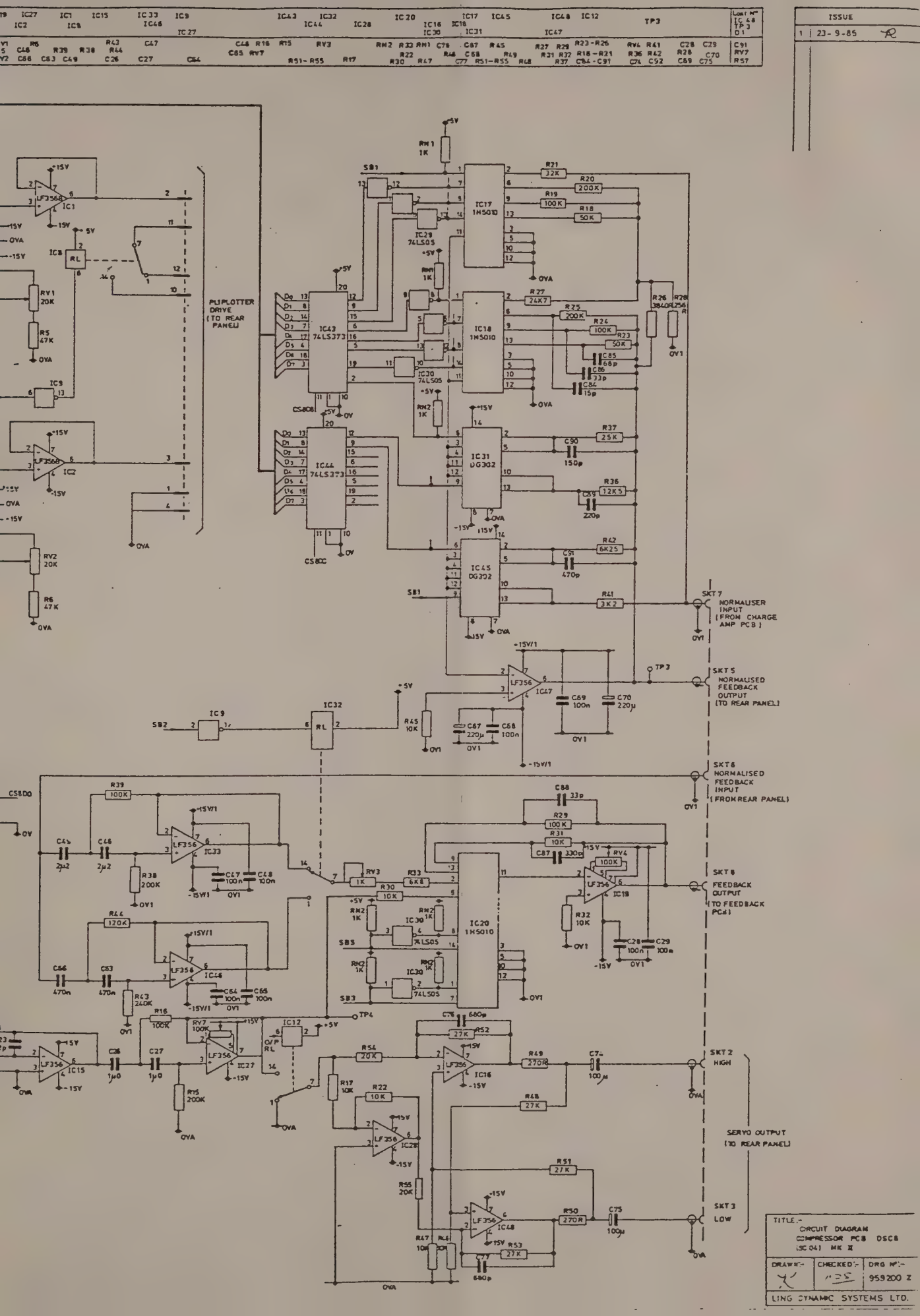
Skt.1 (To Rear Panel)
0VA
Skt.2 Sine Output (To Compressor PCB)

(From Sht.1.)
F DATA
F15 F14 F13 F12 F11 F10 F9 F8 F7 F6 F5 F4 F3 F2 F1 F0

R4 3K0
R5 6K1
R7 12K4
R6 25K
1H5010 IC11
0VA
R8 50K
R9 100K
R11 200K
R10 25K
1H5010 IC12
0VA
R13 50K
R14 100K
R16 200K
R15 25K
1H5010 IC13
0VA
R18 50K
R19 100K
R21 200K
R20 400K
1H5010 IC14
0VA
R22 16R
C35 SOJ
C36 15nF
+15V
IC42 LF356N
-15V
RS9 10K

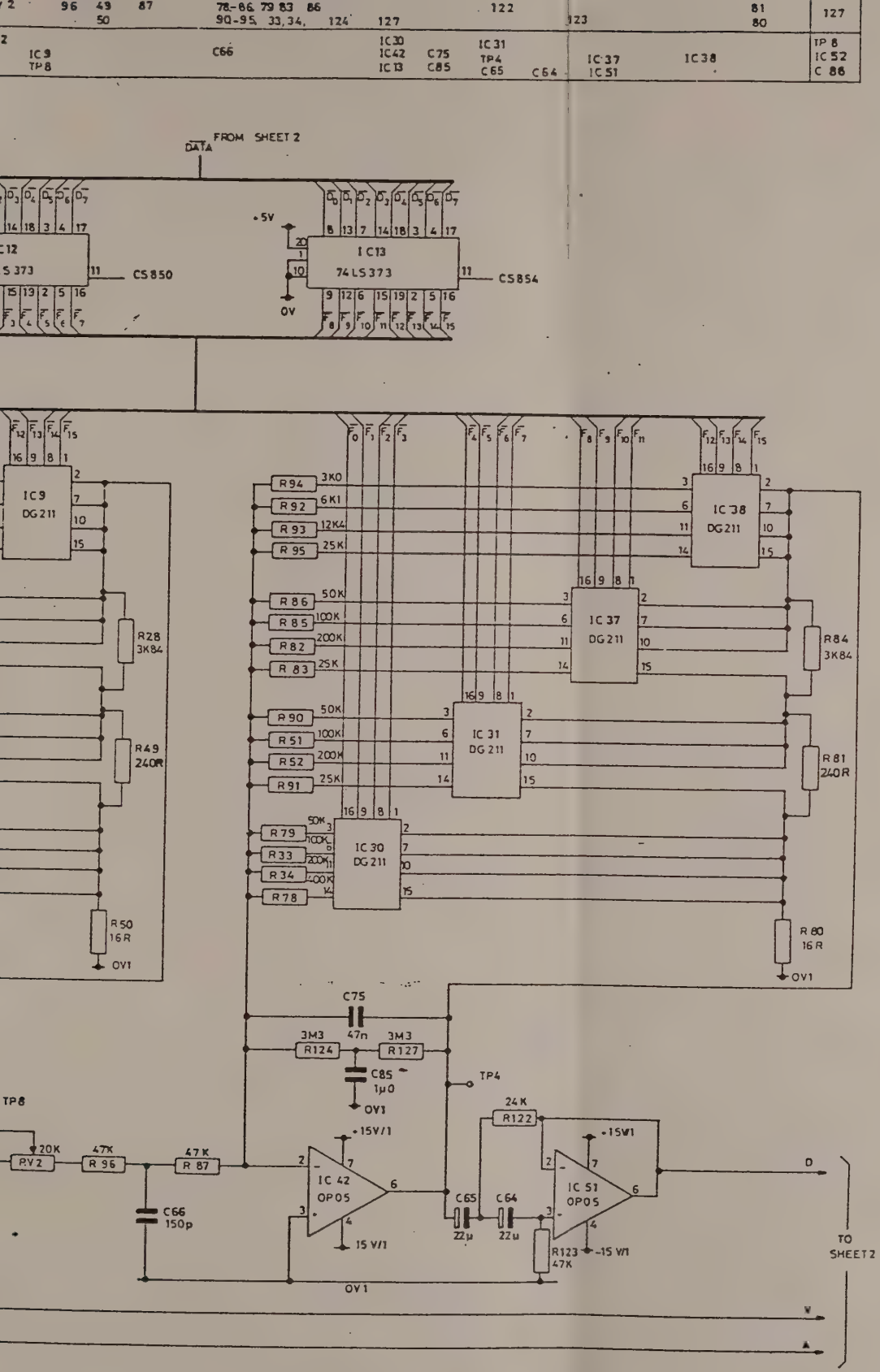
Title		
DSC 8 Sine Generator Circuit Diagram (SC 03) SHT. 2 OF 2		
Drawn JM	Checked MOS	Drg. N° 958140 Y
LING DYNAMIC SYSTEMS LTD		


IC5 IC36 IC22 IC4
DIODES
TPS
RESISTORS R40
CAPACITORS C72 C73 C71
SKT1
INPUT SELECTOR INT. LK
(FROM REAR PANEL)
IC35 PIN 40
IC35 6522 VIA
IC36 8T97
IC22 8T97
IC4 74LS138
IC23 74LS155
IC5 74LS132
IC34 74LS74
IC26 74LS74
IC21 74LS08
IC9 74LS74
IC38 74LS373
IC37 74LS373
IC39 74LS373
IC40 74LS373
IC41 74LS373
IC42 74LS373
IC11 74LS374
IC14 AD7545
IC10 DG 508
IC3 LF356
IC13 LF356
SB1 100mV/g
SB2 5Hz FILTER
SB3 INT. LOOP
SB4 PEN UP
SB5 -20dB TEST
LOW
HIGH
1Hz FILTER
EXT. LOOP
PEN DOWN
0 dB TEST
SKT 4 SINE INPUT (FROM SINE GEN PCB)
DECOUPLING CAPACITORS
22n C1-6, 11, 12, 14-22, 24, 25, 30-45, 50-62, 78-83
IC TYPE
IC N°
0V PIN
+5V PIN
74LS02 IC 6,7 7 14
74LS 05 IC29,30 7 14
74LS 08 IC21 7 14
74LS 74 IC26,34 7 14
74LS132 IC5 7 14


ISSUE
1 | 23-9-85
PLOTTER DRIVE (TO REAR PANEL)
IC1 LF356
IC2 LF356
IC3 LF356
IC8 RL
IC9
IC12
IC15 LF356
IC16 LF356
IC17 1MS010
IC18 1MS010
IC20 1MS010
IC27 LF356
IC28 LF356
IC29 74LS05
IC30 74LS05
IC31 DG302
IC32
IC43 74LS373
IC44 74LS373
IC45 DG302
IC46 LF356
IC47 LF356
IC48 LF356
RV1 20K
RV2 20K
RV3 1K
RV4 100K
RV7 100K
R5 47K
R6 47K
SKT 7 NORMALISER INPUT (FROM CHARGE AMP PCB)
SKT 5 NORMALISED FEEDBACK OUTPUT (TO REAR PANEL)
SKT 6 NORMALISED FEEDBACK INPUT (FROM REAR PANEL)
SKT 8 FEEDBACK OUTPUT (TO FEEDBACK PCB)
SKT 2 HIGH
SKT 3 LOW
SERVO OUTPUT (TO REAR PANEL)
TP3
TP4
TITLE:- CIRCUIT DIAGRAM COMPRESSOR PCB DSCB (SC 041 MK II)
DRAWN:-
CHECKED:-
DRG No:- 959200 Z
LING DYNAMIC SYSTEMS LTD.

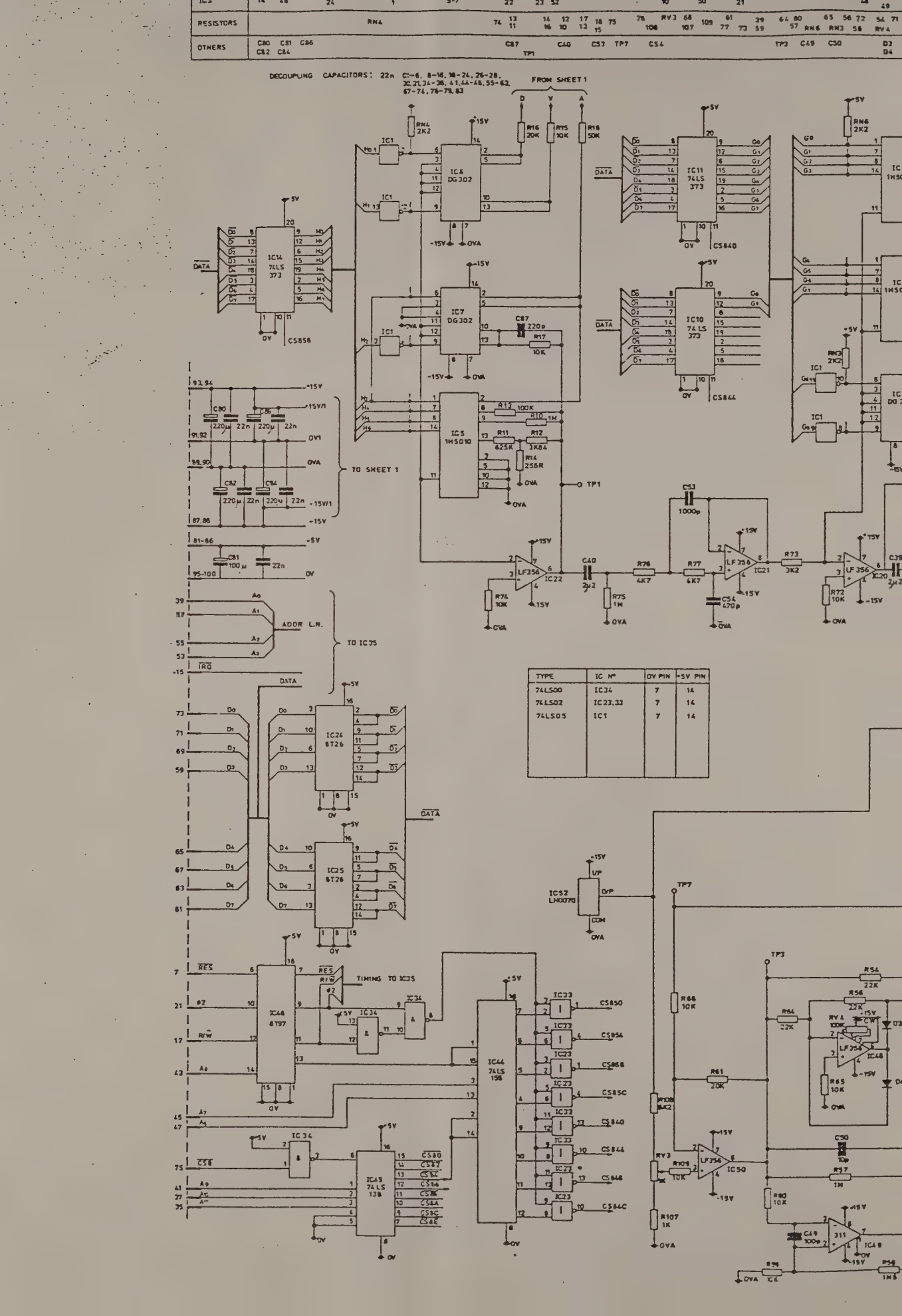
| | | |

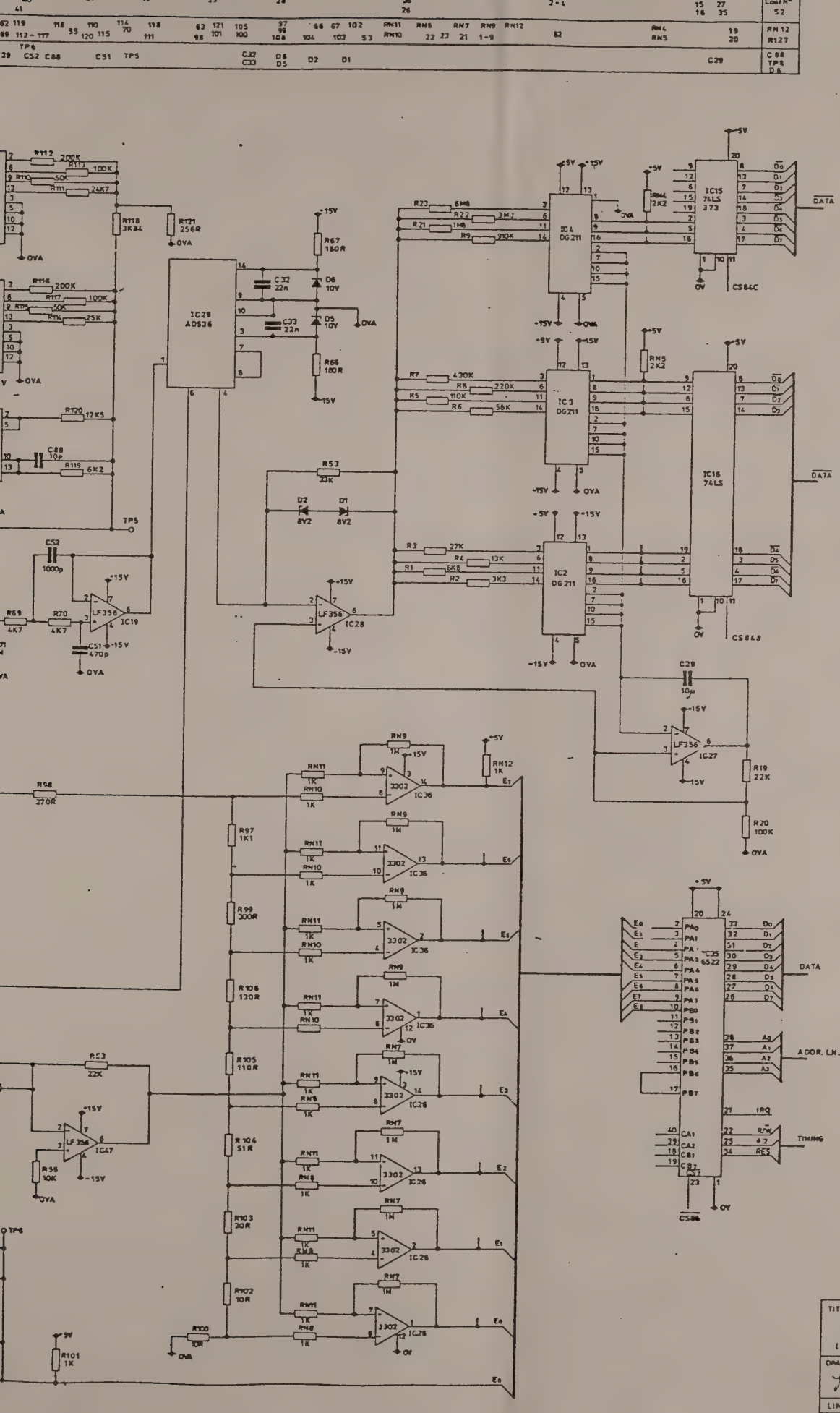
ISSUE		
1	23-9-85	
2	14-11-86 SEE SHT.2.	



SUPPLIES PIN 13 – +15 V1
PIN 12 – + 5 V
PIN 5 – OV1
PIN 4 – -15 V1

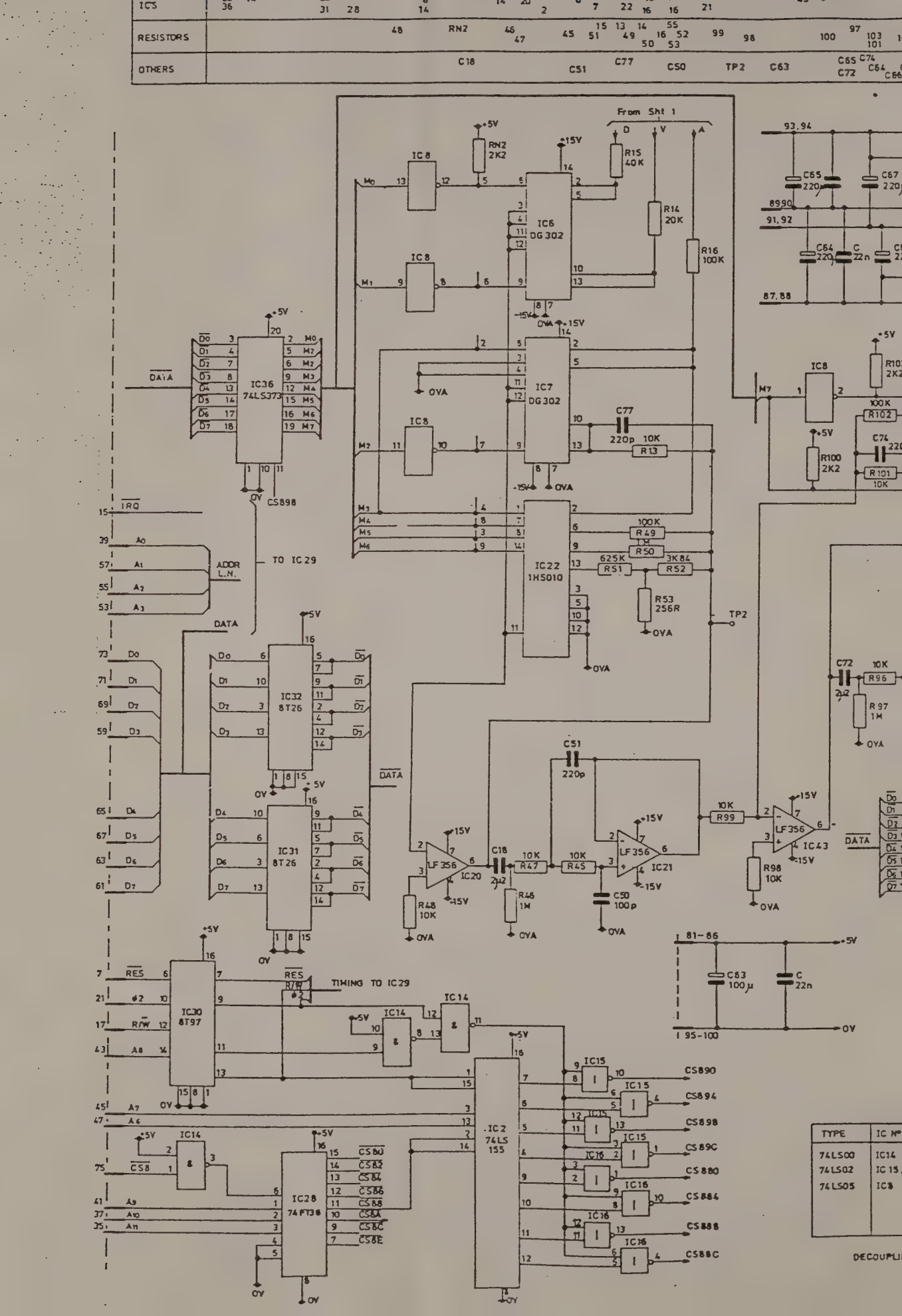
Title		
Circuit Diagram Feedback PCB DSC 8 (SC 05) MKII Sht 1 of 2		
Drawn	Checked	Drg N°
JR	MDS	959210 Y
LING DYNAMIC SYSTEMS LTD		

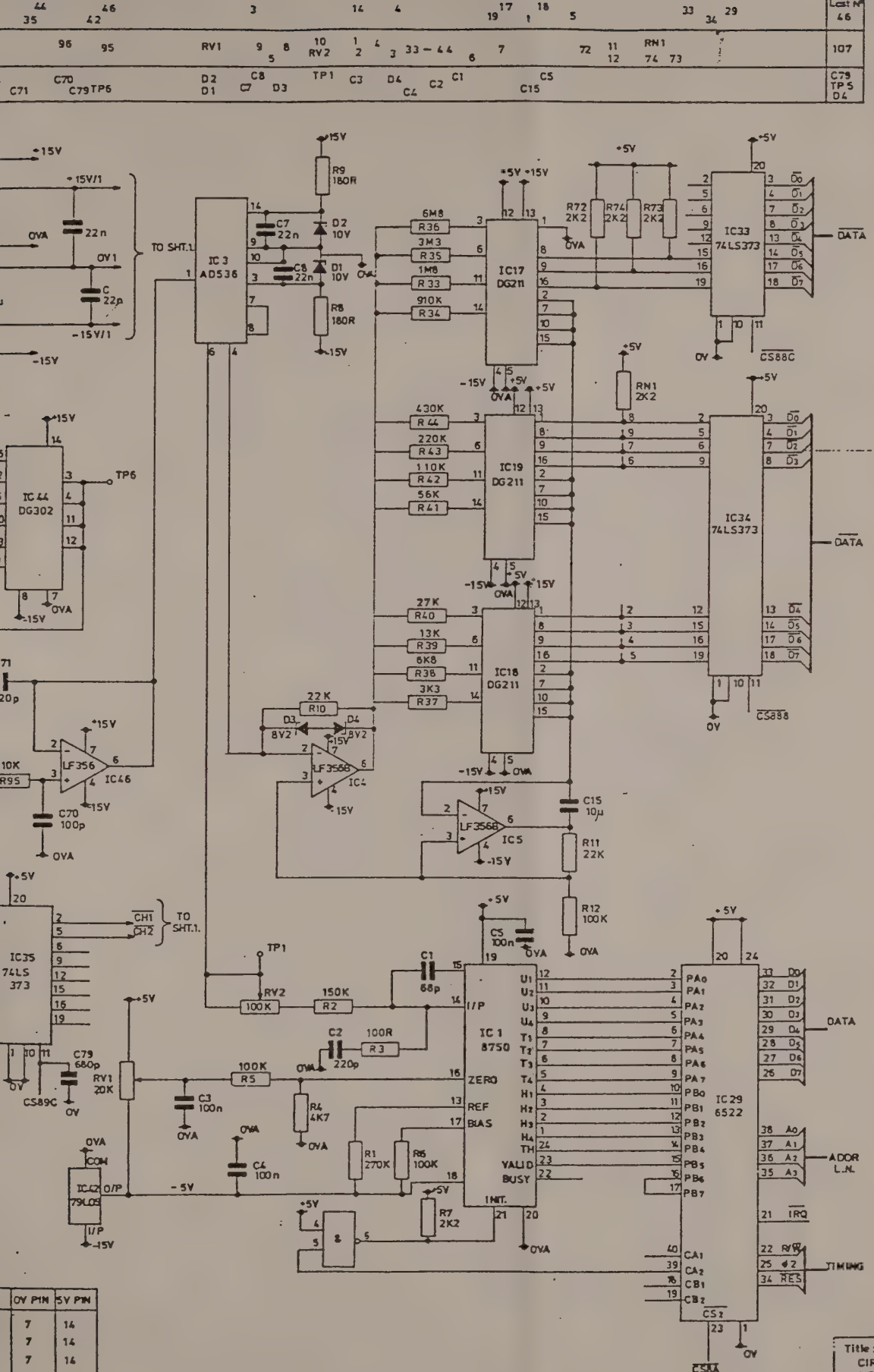

DECOUPLING CAPACITORS: 22n C1-6, 8-16, 18-24, 26-28, 30-31, 34-38, 41, 44-48, 55-62, 67-74, 76-79, 83
FROM SHEET 1
TO SHEET 1
TO IC35
ADDR L.N.
DATA
TIMING TO IC35
TP1
TP3
TP7
CS840
CS844
CS848
CS84C
CS850
CS854
CS858
CS85C
CS880
CS884
CS888
CS88C
CS88E
TYPE
IC N°
0V PIN
+5V PIN
74LS00
IC34
7
14
74LS02
IC23,33
7
14
74LS03
IC1
7
14


ISSUE
1 23-9-85
2 14-11-86 C88 was C87 ECN 3984
IC29 ADS36
IC4 DG211
IC3 DG211
IC2 DG211
IC15 74LS 373
IC16 74LS
IC35 6522
LF356 IC19
LF356 IC28
LF356 IC27
LF356 IC47
3302 IC36
3302 IC26
DATA
ADDR. LN.
TIMING
CS84C
CS84B
CS84A
TITLE:- CIRCUIT DIAGRAM FEEDBACK PCB DSC8 (SCOSI MK II)
SHT 2 OF 2
DRAWN:- R
CHECKED:-
DRG Nº 959210
LING DYNAMIC SYSTEMS LTD

| | | |

| | | |

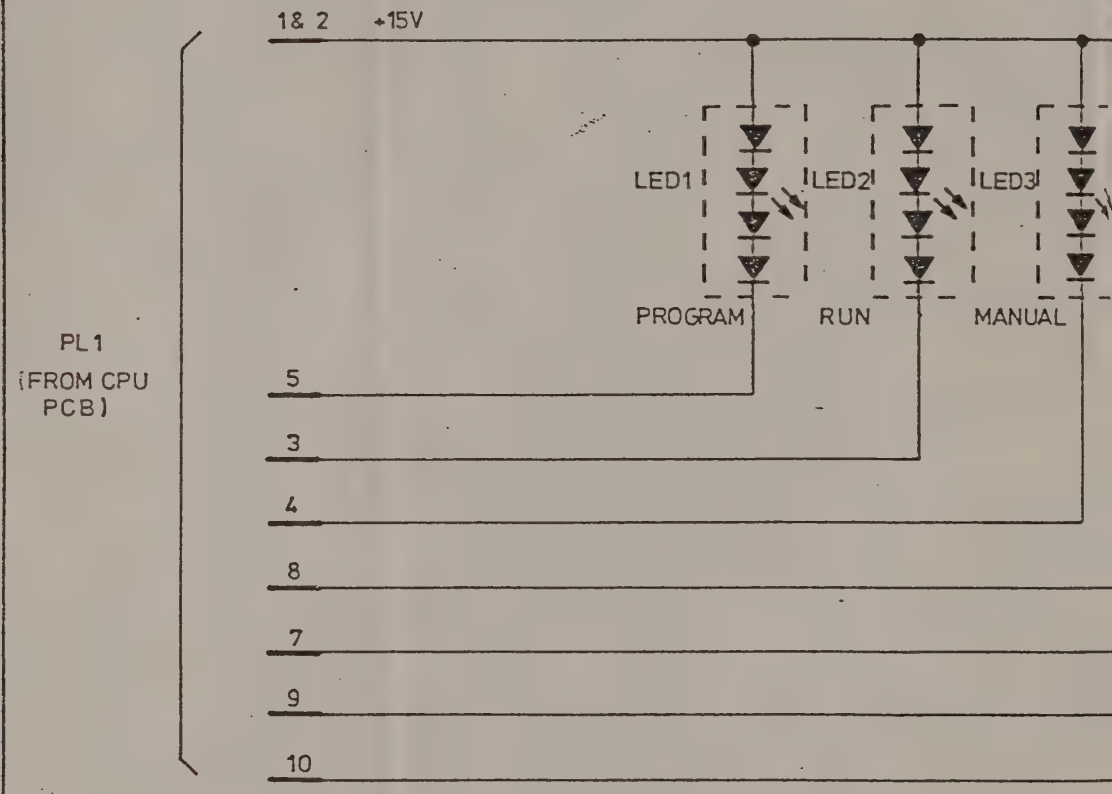

ICS
RESISTORS
OTHERS
From Sht 1
IC8
RN2 2K2
R15 40K
R14 20K
R16 100K
IC6 DG302
IC7 DG302
IC36 74LS373
DATA
IRQ
ADDR L.N.
TO IC29
CS898
C77 220p
R13 10K
IC22 1H5010
R49 100K
R50 TCH
R51 625K
R52 3K84
R53 256R
TP2
IC32 8T26
IC31 8T26
CS1 220p
IC20 LF356
IC21 LF356
IC43 LF356
R47 10K
R45 10K
R46 1M
R48 10K
C50 100p
R99 10K
R98 10K
C72 2µ2
R96 10K
R97 1M
C65 220µ
C67 220µ
C64 220µ
C 22n
C63 100µ
IC30 8T97
RES
TIMING TO IC29
IC14
IC15
IC16
IC2 74LS 155
IC28 74FT38
CS8
CS890
CS894
CS898
CS89C
CS880
CS884
CS888
CS88C
TYPE
IC Nº
74LS00
74LS02
74LS05
DECOUPLI



	0V PIN	5V PIN
	7	14
	7	14
	7	14

CAPACITORS :- 22n, C6, 9-14, 16, 17, 19-21, 23-26, 31, 32 34, 35, 40-49 52-62, 68, 69, 73, 75, 78

DRG. No. 958180	© LING DYNAMIC SYSTEMS LTD., ROYSTON, HERTS, ENGLAND.	OWNS THE CO NOT BE USED



THIRD ANGLE PROJECTION DO NOT SCALE	REMOVE ALL BURRS & SHARP EDGES. MARK PART NUMBER AND ISSUE NUMBER WI

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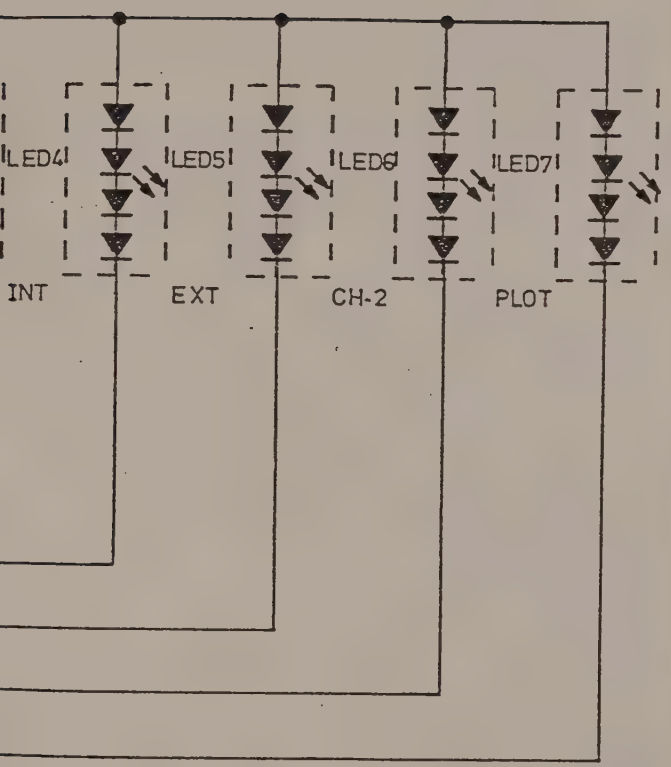


RE SHOWN THUS ⊠

ISSUE		
1	18 – 4 – 84	

USED ON

DATE / /

FOR EXPLANATION OF DIMENSIONS & NOTES ETC SEE B:S 308

ALL DIMENSIONS IN MILLIMETRES

Machine where marked ▽
Surface texture values in μm
Threads are Isometric
Coarse Series
Tolerances Class 6g/6H to B:S 3643

Tolerances unless otherwise Stated
Where one decimal place is shown i.e. 1.5 = ± 0.5
Where two decimal places are sho i.e. 1.50 = ± 0.25
Tolerance on drilled holes ± 1% OR ± 0.05 whichever is grea
Angular tolerance ± 1°

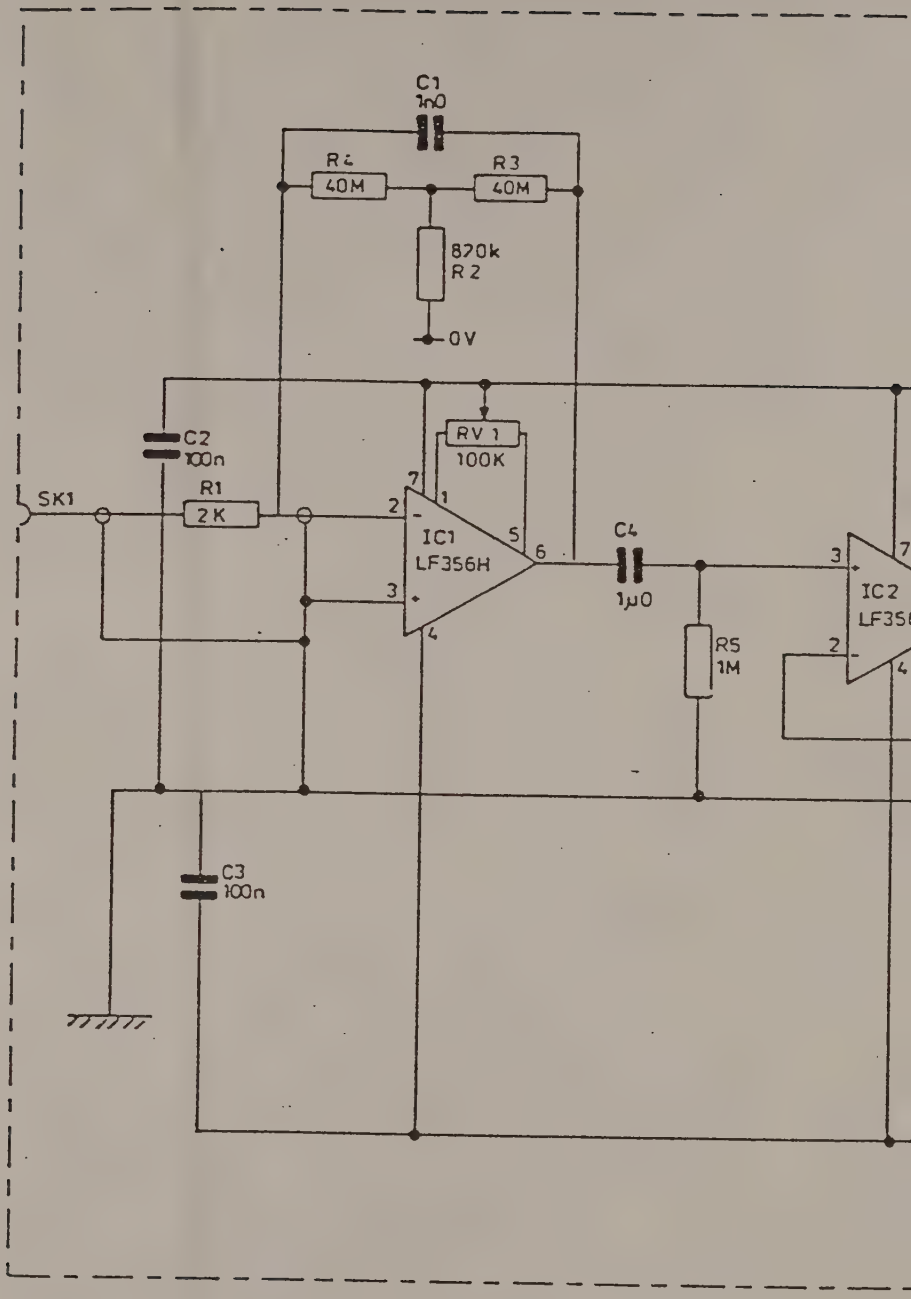
MATERIAL :

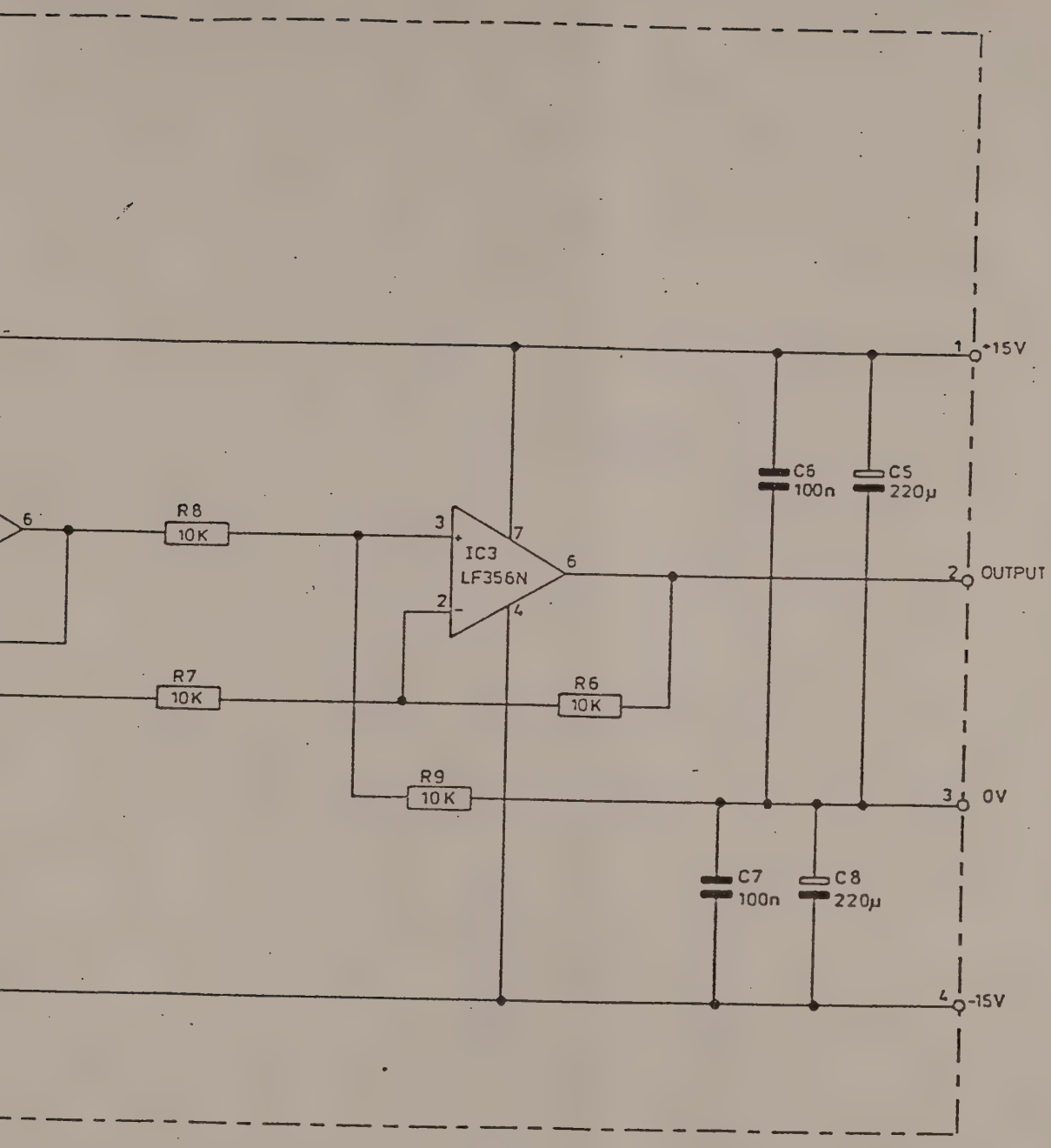
FINISH :

TITLE :

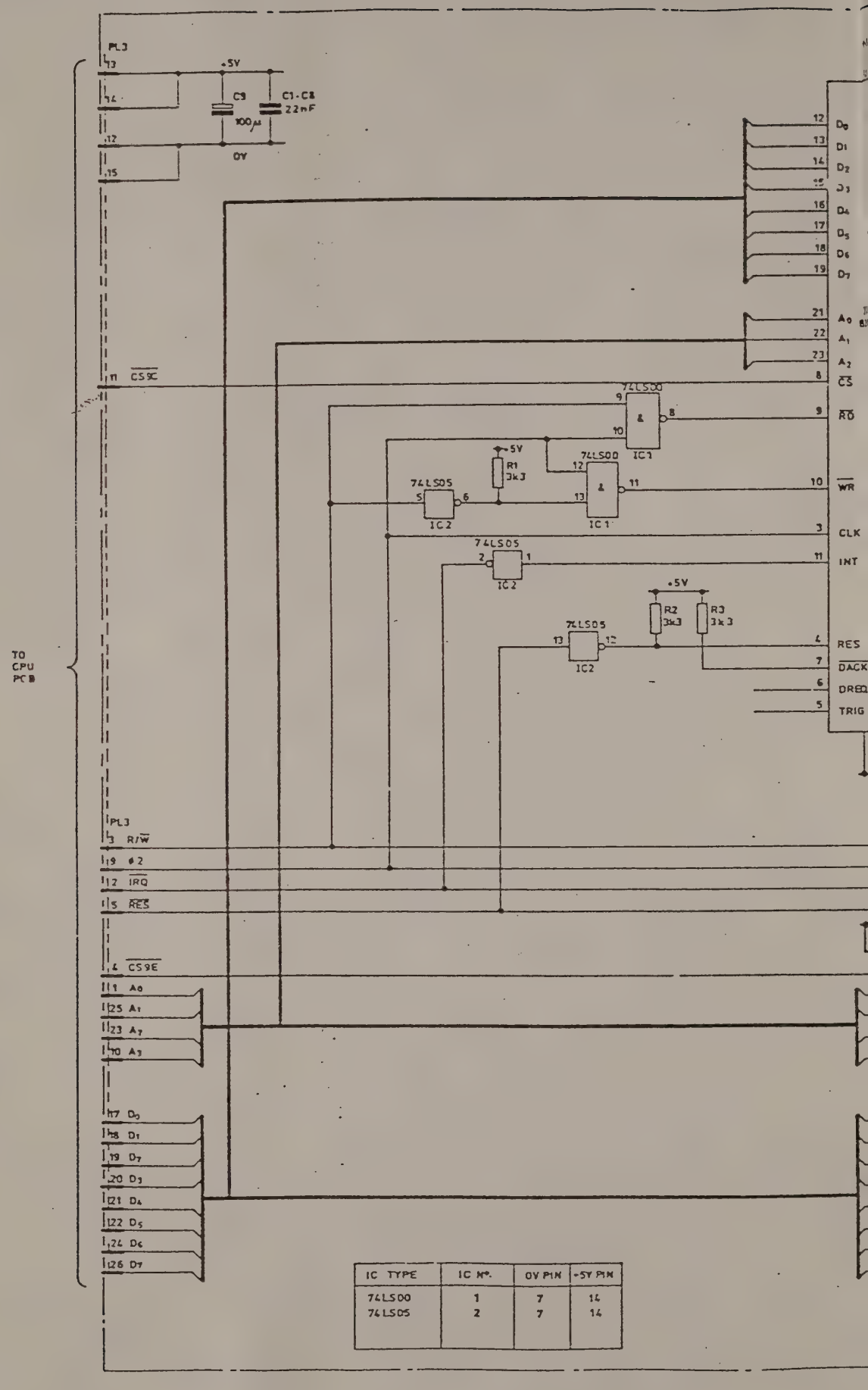
CIRCUIT DIAGRAM STATUS PCB (SCO & DSC 8

DRAWN:	CHECKED:	SCALE:	DRG. No.
JR	MOS		958180

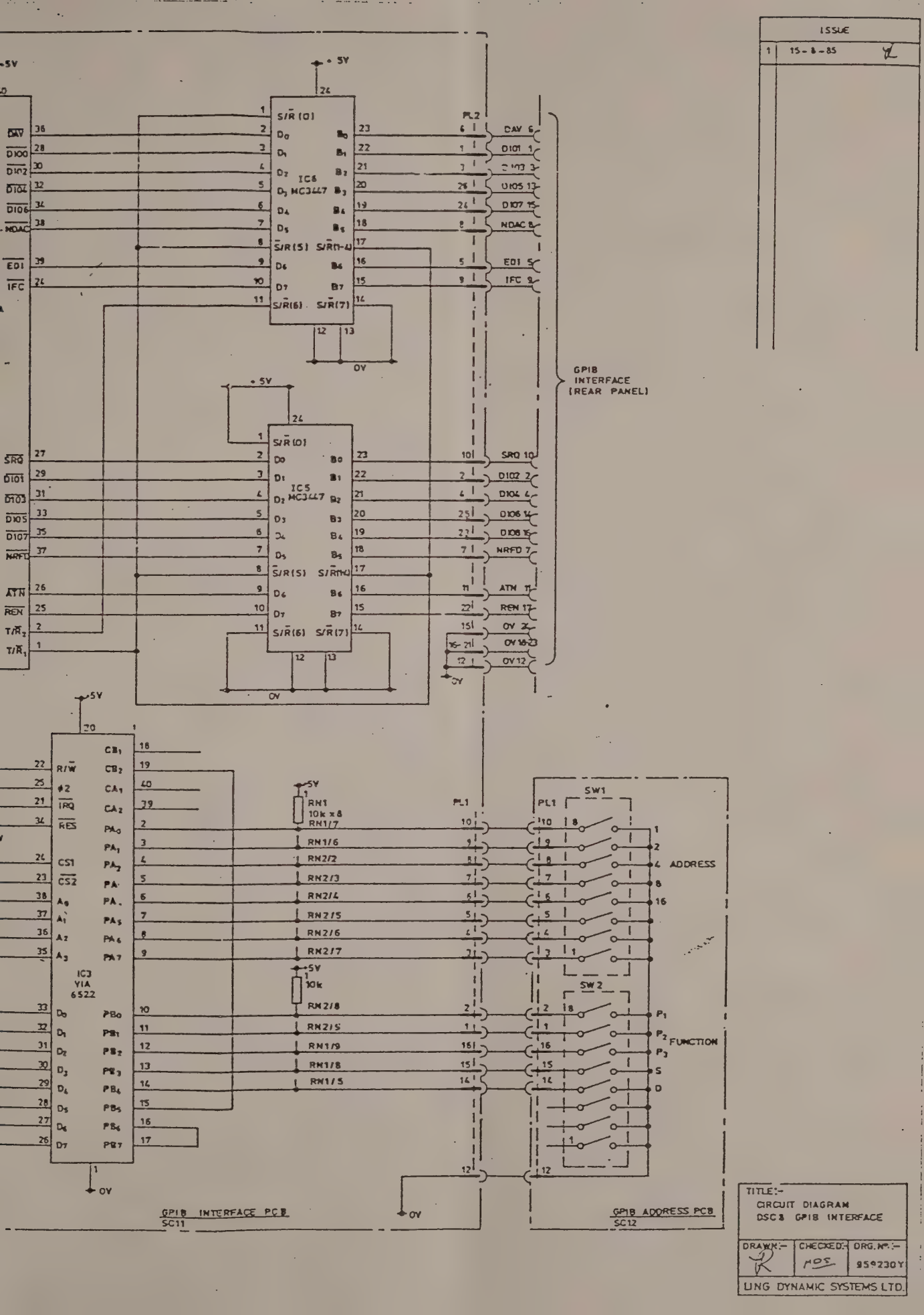

C1
1n0
R4
40M
R3
40M
820k
R2
0V
C2
100n
RV1
100K
CHARGE
INPUT
SK1
R1
2K
IC1
LF356H
C4
1µ0
IC2
LF35
R5
1M
C3
100n



TITLE: Circuit Diagram Charge Amplifier (SC 10) DSC 8		
DRAWN: JR	CHECKED: MOS	DRG Nº: 958610 X
LING DYNAMIC SYSTEMS LTD		



IC TYPE	IC N°.	0V PIN	-5V PIN
74LS00	1	7	14
74LS05	2	7	14


ISSUE
1 15-8-85
+5V
0V
IC6 MC3447
IC5 MC3447
S/R(0)
S/R(1)
S/R(5)
S/R(6)
S/R(7)
S/R(4)
PL2
DAV 6
D101 1
D103 3
D105 13
D107 15
NDAC 8
EOI 5
IFC 9
SRQ 10
D102 2
D104 4
D106 14
D108 16
NRFD 7
ATN 11
REN 17
GPIB INTERFACE (REAR PANEL)
IC3 VIA 6522
RN1 10k x8
RN1/7
RN1/6
RN2/2
RN2/3
RN2/4
RN2/5
RN2/6
RN2/7
RN2/8
RN2/5
RN1/9
RN1/8
RN1/5
10k
PL1
SW1
SW2
ADDRESS
FUNCTION
GPIB INTERFACE PCB
SC11
GPIB ADDRESS PCB
SC12
TITLE:-
CIRCUIT DIAGRAM
DSC8 GPIB INTERFACE
DRAWN:-
CHECKED:-
MOS
ORG.NO:-
959230Y
LING DYNAMIC SYSTEMS LTD.

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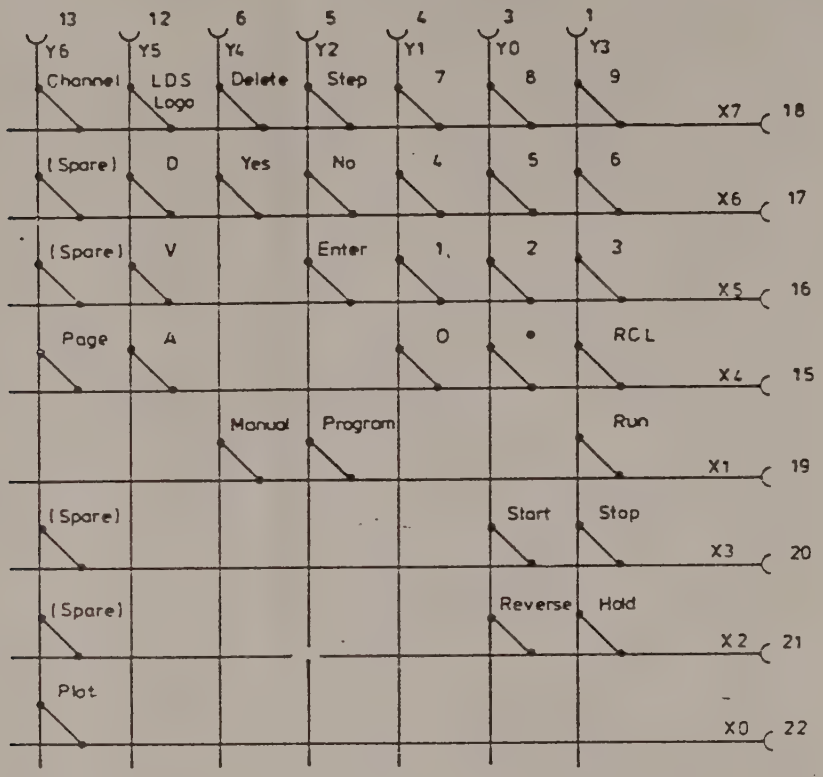
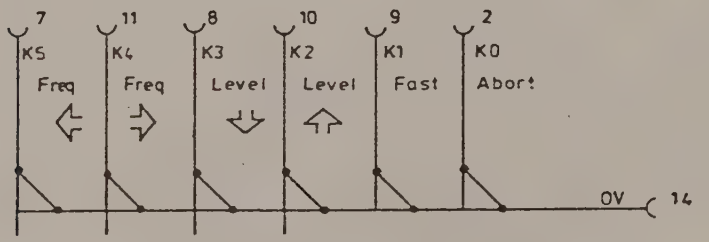
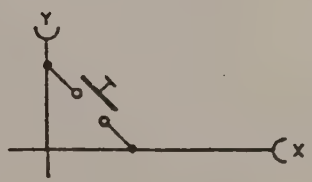
ROYSTON, HERTS,







Detail
Used

RD ANGLE PROJECTION
DO NOT SCALE

REMOVE ALL BURRS & SHARP EDGES
MARK PART NUMBER AND ISSUE NUMBER WHERE SHOWN THUS

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ISSUE		
1	13 - 2 - 84	

USED ON

DATE / /

Of Switch
41 Positions

FOR EXPLANATION OF DIMENSIONS & NOTES ETC SEE B:S 308

ALL DIMENSIONS IN MILLIMETRES

Machine where marked ✓
Surface texture values in μm
Threads are Isometric
Coarse Series
Tolerances Class 6g/6H to B:S 3643

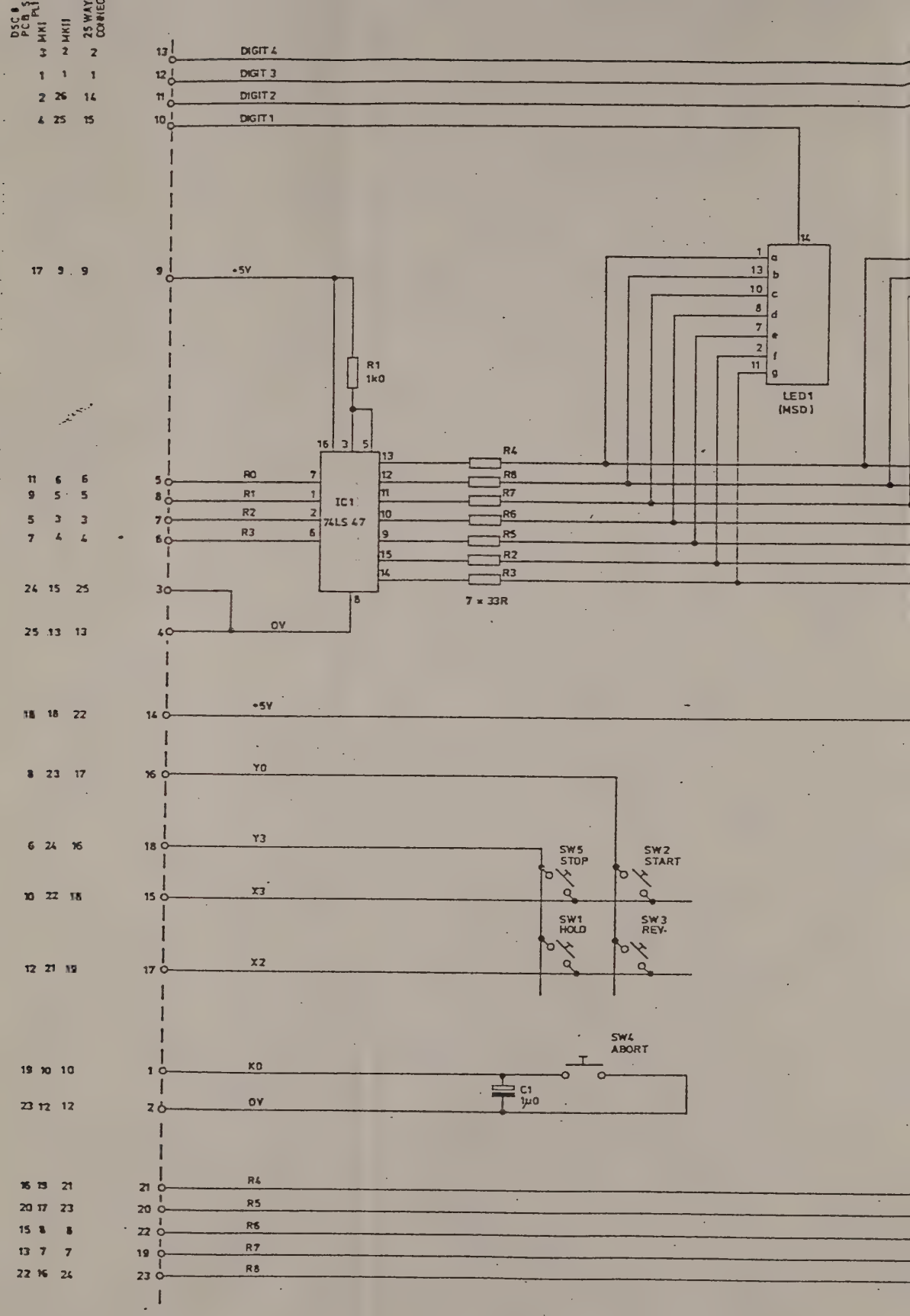
Tolerances unless otherwise Stated
Where one decimal place is shown i.e. 1.5 = ± 0.5
Where two decimal places are shown i.e. 1.50 = ± 0.25
Tolerance on drilled holes ± 1% OR ± 0.05 whichever is greater
Angular tolerance ± 1°

MATERIAL:

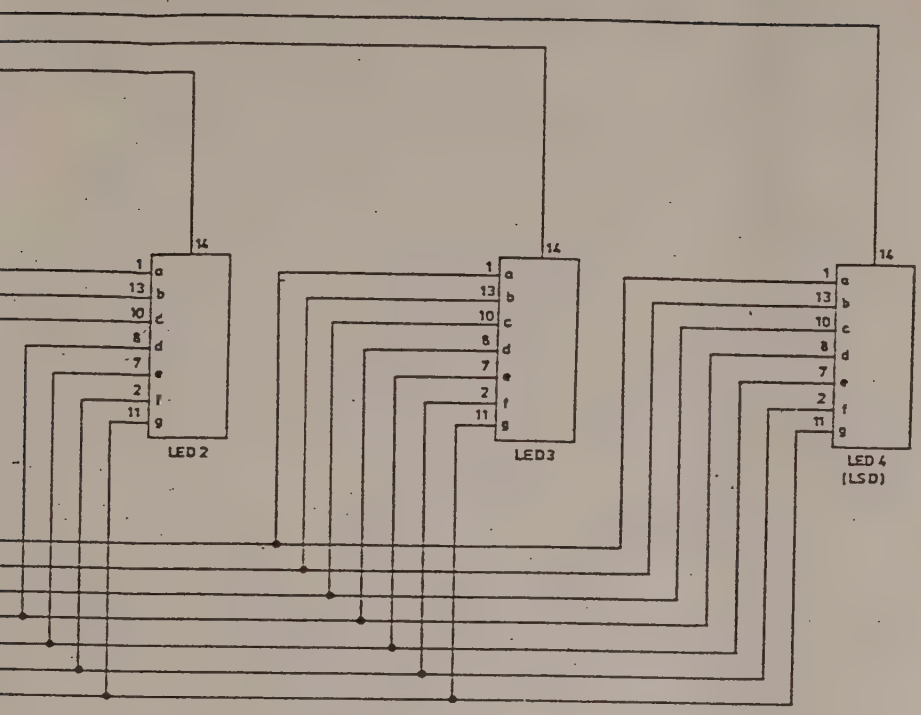
FINISH:

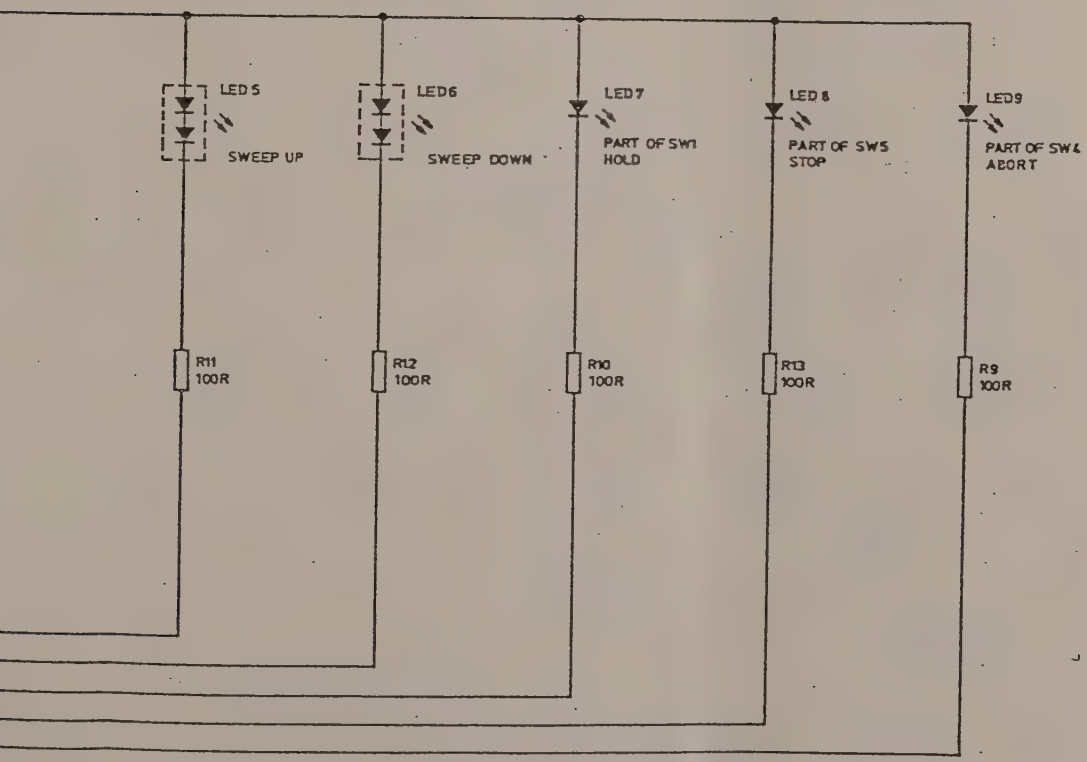
TITLE: CIRCUIT DIAGRAM KEYBOARD DSC 8

DRAWN:	CHECKED:	SCALE:	DRG. No.
	MOS		958750 X


DSC ⊕ PCB SKT PLT
MKI MKII 25 WAY CONNECTOR
DIGIT 4
DIGIT 3
DIGIT 2
DIGIT 1
+5V
R1 1k0
IC1 74LS 47
R0
R1
R2
R3
R4
R5
R6
R7
R8
7 × 33R
LED1 (MSD)
0V
+5V
Y0
Y3
X3
X2
SW5 STOP
SW2 START
SW1 HOLD
SW3 REV.
SW4 ABORT
K0
0V
C1 1µ0
R4
R5
R6
R7
R8

ISSUE		
1	6-9-84	R
2	28-10-85 CPU PCB PL1 PIN NOS FOR DSC8 MKII ADDED ECN 3476	R

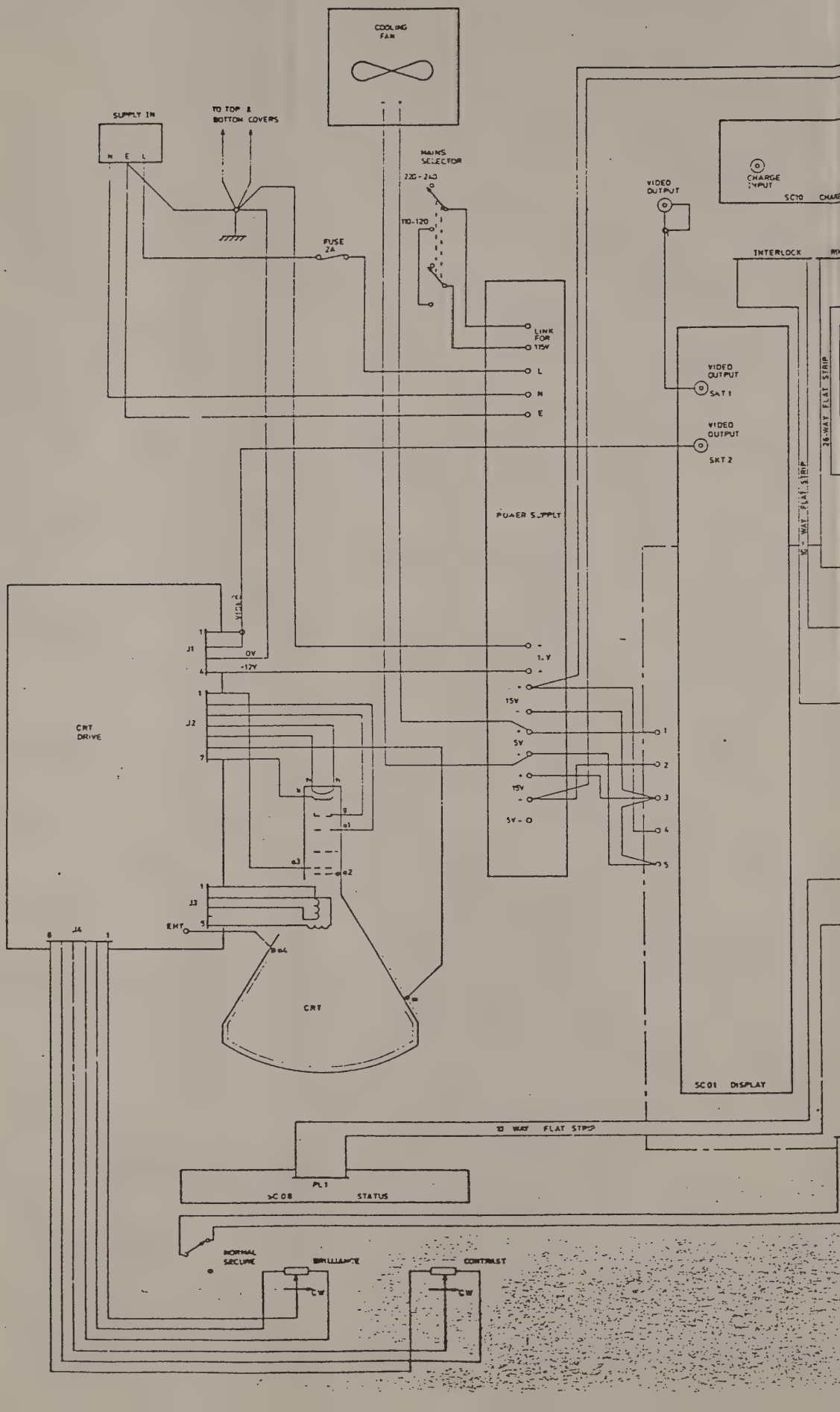


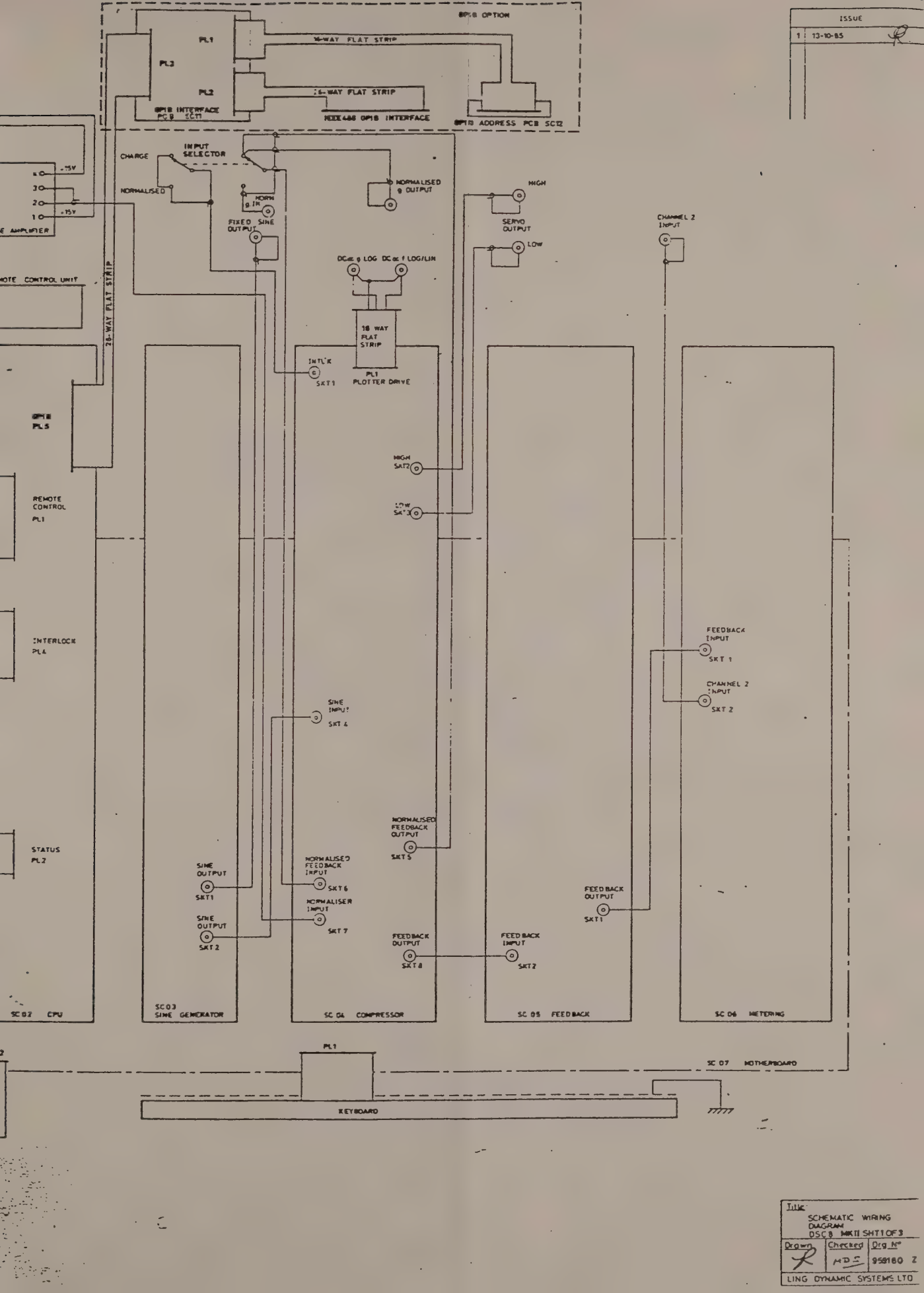


Title:
CIRCUIT DIAGRAM
REMOTE CONTROL UNIT
(DSC8)

Drawn:	Checked:	Drg N° :
R		958660 Y

LING DYNAMIC SYSTEMS LTD


COOLING FAN
SUPPLY IN
N E L
TO TOP & BOTTOM COVERS
MAINS SELECTOR
220-240
110-120
FUSE 2A
LINK FOR 115V
L
N
E
VIDEO OUTPUT
CHARGE INPUT
SC10
INTERLOCK
VIDEO OUTPUT SKT 1
VIDEO OUTPUT SKT 2
26-WAY FLAT STRIP
POWER SUPPLY
VISIC
J1
0V
-12V
1.Y
15V
5V
15V
5V-0
CRT DRIVE
J2
J3
EHT
J4
CRT
SC01 DISPLAY
10 WAY FLAT STRIP
PL1
SC08 STATUS
NORMAL SECURE
BRILLIANCE
CONTRAST
CW
CW



Title: SCHEMATIC WIRING DIAGRAM DSC8 MKII SHT1 OF 3		
Drawn	Checked	Drg N°
	MDS	959180 Z

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39	A0	
40	Y7	NOT USED
41	A9	
42	Y8	NOT USED
43	A8	
44	Y9	NOT USED
45	A7	
46	Y10	NOT USED
47	A6	
48	K2 (LEVEL UP)	10
49	A5	
50	K3 (LEVEL DOWN)	8
51	A4	
52	FAST	9
53	A3	
54	K5 (FREQ DOWN)	7
55	A2	
56	K4 (FREQ UP)	11
57	A1	
58	FAST	9
59	D3	
60	V SYNC	
61	D7	
62	FREQ x 64	
63	D6	
64		
65	D4	
66		
67	D5	
68		
69	D2	
70		
71	D1	
72		
73	D0	
74		
75	$\overline{CS8}$	
76		
77	$\overline{CS9}$	
78		
79	$\overline{CSA}$	
80		
81	+ 5 VOLTS	
82	+ 5 VOLTS	
83	+ 5 VOLTS	
84	+ 5 VOLTS	
85	+ 5 VOLTS	
86	+ 5 VOLTS	
87	- 15 VOLTS	
88	- 15 VOLTS	
89	OV (ANALOGUE)	
90	OV (ANALOGUE)	
91	OV (INPUT)	
92	OV (INPUT)	
93	+ 15 VOLTS	
94	+ 15 VOLTS	
95	OV (DIGITAL)	
96	OV (DIGITAL)	
97	OV (DIGITAL)	
98	OV (DIGITAL)	
99	OV (DIGITAL)	
100	OV (DIGITAL)	

SCO2 PL4	FUNCTION	REAR PANEL INTERLOCK 'D' SKT
1	START (↑) STOP (↓)	1
2	RELAY CONTACT	2 CLOSE ON START
3	RELAY CONTACT	3 OPEN ON SHUTDOWN
4	INHIBIT (↑)	4
5	EXT ABORT (↓)	5
6	REVERSE (↓)	13
7	HOLD (↓)	12
8	0 VOLTS	11
9	0 VOLTS	10
10	0 VOLTS	9

STATUS

SCO PL2	FUNCTION	SCO8 PL1
1	+ 15 VOLTS	1
2	RUN LED	2
3	PROGRAM LED	3
4	EXT LOOP LED	4
5	CH2 LED	5
6	PLOT LED	6
7	INT LOOP LED	7
8	-	8
9	MANUAL LED	9
10	+ 15 VOLTS	10

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DRAG No. 951180

REMOVE ALL BURRS & SHARP EDGES
MARK PART NUMBER AND ISSUE NUMBER WHERE SHOWN THUS

THIRD ANGLE PROJECTION
DO NOT SCALE

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ISSUE		
1	24-10-85	

USED ON

DATE

FOR EXPLANATION OF DIMENSIONS & NOTES ETC SEE B:S 308

ALL DIMENSIONS IN MILLIMETRES

Machine where marked ▽

Surface texture values in μm

Threads are Isometric

Coarse Series

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Angular tolerance ± 1°

MATERIAL:

FINISH:

TITLE: SCHEMATIC WIRING DIAGRAM DSC 8 MK II SHT 2 OF 3

DRAWN:

CHECKED: MDS

SCALE:

DWG. No. 959180

X

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MOTHER BOARD

SK 1-6 EDGE CONNECTOR	FUNCTION	PL1 KEYBOARD
1		
2		
3		
4		
5		
6		
7	$\overline{RES}$	
8	KO (ABORT)	2
9	SO	
10	Y2	5
11	$\overline{NMI}$	
12	Y1	4
13	RDY	
14	YO	3
15	$\overline{IRQ}$	
16	X7	18
17	R/$\overline{W}$	
18	X6	17
19	$\overline{DMA}$	
20	X5	16
21	Ø2	
22	X4	15
23	Ø1	
24	X3	20
25	SYNC	
26	X2	21
27	A12	
28	X1	19 (VIA PL2 - KEYSWITCH)
29	A15	
30	XO	22
31	A14	
32	Y3	1
33	A13	
34	Y4	6
35	A11	
36	Y5	12
37	A10	
38	X6	13

FLAT STRIP ASSEMBLY CONNEXIONS

REMOTE CONTROL

SCO2 PL1	FUNCTION	REAR PANEL REMOTE CONTROL UNIT 'D' SKT	REMOTE CONTROL UNIT PCB PIN No.
1	DIGIT 3	1	12
2	DIGIT 4 (LSD)	2	13
3	DISPLAY B2	3	7
4	DISPLAY B3	4	6
5	DISPLAY B1	5	8
6	DISPLAY BO	6	5
7	STOP LED	7	19
8	HOLD LED	8	22
9	+ 5 VOLTS	9	9
10	KO (ABORT)	10	1
11	-	11	-
12	0 VOLTS	12	2
13	0 VOLTS	13	4
14	-	-	-
15	0 VOLTS	25	3
16	ABORT LED	24	23
17	SWEEP DOWN LED	23	20
18	+ 5 VOLTS	22	14
19	SWEEP UP LED	21	21
20	-	20	-
21	X2	19	17
22	X3	18	15
23	YO	17	16
24	Y3	16	18
25	DIGIT 1 (MSD)	15	10
26	DIGIT 2	14	11

INTERLOCK

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ROYSTON

DRG. No. 959180

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1	24-10-85

PLOTTER

SC04 PL1	FUNCTION	REAR PANEL PLOTTER 'D' SKT
1	0 VOLTS	1
2	DC	2
3	DC	3
4	0 VOLTS	4
5	-	5
6	-	6
7	-	7
8	-	8
9	-	-
10	PEN LIFT N.O.	15
11	PEN LIFT COMMON	14
12	PEN LIFT N.C.	13
13	-	12
14	-	11
15	-	10
16	-	9

CPU - GPIB

SC02 PL5	FUNCTION	SC11 PL3
1		1
2		2
3		3
4	A0	4
5	IRQ	5
6	R/W	6
7	CS 9E	7
8	RES	8
9	-	9
10	-	10
11	ø2	11
	A3	
	CS 9C	

GPIB I/O

SC11 PL2	FUNCTION	REAR PANEL GPIB SOCKET
1	DIO 1	1
2	DIO 2	2
3	DIO 3	3
4	DIO 4	4
5	EOI	5
6	DAV	6
7	NRFD	7
8	NDAC	8
9	IFC	9
10	SRQ	10
11	ATN	11
12	0V (SCREEN)	12
13	-	-
14	-	-
15 - 21	0 VOLTS	24 - 18
22	REN	17
23	DIO8	16
24	DIO7	15
25	DIO6	14
26	DIO5	13

GPIB ADDRESS

SC11 PL1	FUNCTION	SC12 PL1

USED ON

DATE / /

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Angular tolerance ± 1°

MATERIAL:

FINISH:

TITLE:
SCHEMATIC WIRING DIAGRAM
DSC 8 MKII
SHT. 3 OF 3

DRAWN:	CHECKED:	SCALE:	DRG. No.
K	MDS		959180

MP MASTER
MA34247